Multi-objective Design of Hardware Accelerators for Levodopa-Induced Dyskinesia Classifiers

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Abstract. Taking levodopa, a drug used to treat symptoms of Parkinson's disease, is often connected with severe side effects, known as Levodopa-induced dyskinesia (LID). It can fluctuate in severity throughout the day and thus is difficult to classify during a short period of a physician's visit. A low-power wearable classifier enabling long-term and continuous LID classification would thus significantly help with LID detection and dosage adjustment. This paper deals with a co-evolutionary design of energy-efficient hardware accelerators of LID classifiers that can be implemented in wearable devices. The accelerator consists of a feature extractor and a classifier co-evolved using cartesian genetic programming (CGP). We introduce and evaluate a fast and accurate energy consumption estimation method for the target architecture of considered classifiers. The proposed energy estimation method allows for a multi-objective design enabled by introducing energy constraints. With the introduction of variable data representation bit width, the proposed method achieves a good trade-off between accuracy (AUC) and energy consumption.

Keywords: Cartesian genetic programming · Multi-objective design · Hardware accelerator · Energy-efficient · Levodopa-induced dyskinesia.

1 Introduction

Parkinson's disease (PD) is one of the most common neurological conditions affecting the motor system. Patient care primarily suppresses symptoms using a *levodopa* drug, which can result in *levodopa-induced dyskinesia* (LID). A wearable device allowing long-term continuous LID classification would be a great source of information and help physicians adjust the dosage to suppress PD symptoms and, at the same time, reduce LID.

Lones et al. [4] proposed a LID-classifier model utilising a sliding window of 32 samples of low-level movement features and designed it using *genetic programming* (GP). Hurta et al. [3] further adopted this model for hardware implementation and used *cartesian GP* (CGP) [6] for the evolutionary design of an energy-efficient *feature extractor* (FE). The FE and classifier design – as a complex problem – was solved using a co-evolution approach. Their model also reduced data representation to an 8-bit integer.

The evolution design in [3] is guided only by the solution accuracy in terms of AUC (Area Under the receiver operating characteristics Curve). The number of arithmetic operations was used to estimate the hardware complexity of the final solutions. Only the best classifiers were selected and synthesised for the final evaluation. Moreover, existing works do not consider the sub-byte arithmetics, even though the sub-byte operations are currently successfully used in neural networks and machine learning accelerators [7].

To address these challenges, we propose an improved co-evolutionary design method. Our method allows for sub-byte data representation by encoding bit-width inside candidate solutions. Further, we propose an effective way of precise energy estimation during the evolution process and utilise it in a multi-objective design. Multi-objective design is achieved by transforming the multi-objective problem into a single-objective one by introducing constraints [5].

2 Proposed Methodology

The FE and classifier models are based on a co-evolutionary scheme proposed by Hurta et al. [3]. FE and classifier are designed simultaneously by switching the currently-evolved *population* in each epoch. Populations interact through the evaluation phase, where candidate solutions of one population are evaluated in connection with the currently best candidate solution from the other population. The *fitness* of *candidate solutions* is given as the composition's classifier accuracy (AUC). Data from the clinical study [4] is used for the fitness calculation. We also implement the co-evolution of *Adaptive Size Fitness Predictors* (ASFP) [1] that accelerates evolution.

The selection of the bit width of individual parts (i.e. FE and classifier) is incorporated into the evolution process. Bit widths are included inside the candidate solutions' chromosomes and evolve together with the cartesian grid representing the evolved program. The value of bit width spans from 3 to 12 bits and is mutated with probability equal to its portion of the chromosome.

Calculation of energy consumption traditionally involves a computationally expensive synthesis of each candidate solution. To eliminate this issue, we propose to use pre-synthesised components. Hence, we designed and synthesised each combination of 18 allowed functions and ten possible values of bit widths. This results in a look-up table of 180 different possible values of energy consumption. As the LID classifier comprises up to 32 registers, a similar table is

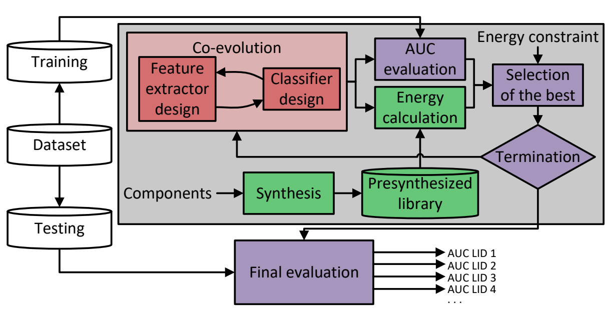

Fig. 1. Overview of the proposed multi-objective method for the co-evolutionary design of energy-efficient LID classifier.

also created for ten different bit widths of registers. Further, as classifiers generally do not utilise full sliding windows, we propose the elimination of unrequired circuits to reduce energy consumption.

The proposed solution of multi-objective design involves transforming a multi-objective problem into a single-objective. The evolution of candidate solutions is guided by the objective of classification accuracy (AUC). The objective of energy consumption is transformed into constraint ε. The fitness f of the candidate solution (the composition of feature extractor FE and classifier C) is equal to the achieved accuracy $AUC(FE, C)$ only if the energy consumption $E(FE, C)$ is lower than ε. In the opposite case, fitness f is given as $-E(FE, C)$. This fitness function allows the method to improve even energy-unfit candidate solutions, which may happen especially in first generations. Combining solutions from runs with different constraints ε allows for obtaining solutions spanning a wide range of energy consumption requirements while maintaining the goal of high precision and thus achieving a wide Pareto front. The overview of the proposed method is shown in Fig. 1.

3 Results

The adopted parameter settings are based on the settings proposed by Hurta et al. [3]. The evolutionary strategy $(1 + \lambda)$ was employed together with a limit of 10,000 generations, a grid size of 4x8 and the Goldman mutation operator [2]. One hundred independent runs of each parameter setting were performed to allow precise evaluation. Energy consumption of individual components was synthesised with Synopsys Design Compiler targeting 45 nm ASIC technology on 100 MHz frequency.

Introducing the variable width requires checking whether the maximum fitness can still be reached. For this reason, a comparison of the baseline variant with a fixed 8-bit width and the variable variant was made. Mann-Whitney U-test confirmed a non-significant difference between both variants for all test groups of the data set except LID1 and Sitting, where improvement was achieved. Modifying the initialization in the initial population from 8-bit width to a random value (in the range of 3-12) led to an additional improvement across most test groups (except for test group LID1), with a significant improvement in test groups LID3 and Siting.

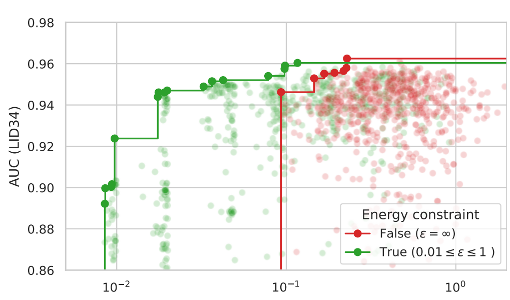

Fig. 2. Trade-offs between energy consumption and AUC on test group LID34. Green represents solutions obtained by a union of 100 runs for each of the seven selected energy constraints. Red represents 700 runs of the method without energy constraint.

To obtain a rich Pareto front, 100 independent runs were performed for each of seven logarithmically distributed energy constraint values from 0.01 pJ to 1 pJ. To conduct a fair comparison with the standard variant, 700 independent runs with unconstrained energy consumption (i.e., $\varepsilon = \infty$) were also performed. Fig. 2 compares Pareto fronts obtained by combining the results of different energy constraint settings and the standard variant. The Pareto front achieved by the method utilizing the combined energy constraints dominates most space. In contrast, the variant without energy constraints is better only in finding a solution with the highest AUC.

4 Conclusions

In this paper, we proposed a method for the multi-objective design of HW accelerators for LID classifiers. The proposed efficient energy consumption estimation allowed us to include energy consumption directly into the evolution process and solve the multi-objective design problem (with a trade-off between accuracy and energy consumption) by introducing constraints on energy consumption and thus transforming it into a single-objective problem. With the introduction of variable bit width, proposed improvements allowed the design of a wide range of high-quality solutions achieving a good trade-off between accuracy and energy consumption.

Acknowledgements This work was supported by the Czech Science Foundation project 21-13001S and BUT Internal Grant Agency through project FIT-S-23-8141. The computational resources were supported by the MSMT project e-INFRA CZ (ID:90140). We also acknowledge Prof. Stephen Smith and Dr Michael Lones for their advice; Dr Jane Alty, Dr Jeremy Cosgrove, and Dr Stuart Jamieson for their contribution to the clinical study that generated the data, and the UK National Institute for Health Research (NIHR) for adopting the study within in its Clinical Research Network Portfolio.

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