Educational Toolset for Experimenting with Optimizations in the Area of Cost/Quality Trade-Offs Related to Digital Circuit Diagnosis

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Abstract

The paper presents a toolset utilizable for learning and training principles related to design-for-testability of digital systems by means of structural and ad-hoc techniques. Actually, the toolset consists of two tools named SET and CADeT. Using the tools, user is allowed to make experiments in the optimization area which goal is to achieve feasible cost/quality trade-off among design-constraints and diagnostic requirements posed on a digital system. In the paper, basic education-related characteristics of the tools are briefly presented.

SET tool

SET (*Scan Educational Tool*) consists of *testability*[1] *analysis* (*TA*) module and *scan technique*[2] *application* (*SA*) module. The goal of TA module developed on basis of TA method presented in [1] is to perform, evaluate and display testability results of an *educational circuit*[3] according to user-selected *scan-layout*[4]. The goal of SA module is to automatically find such a scan-layout that meets selected design constraints the most (actually, area and pin overhead constraints are supported).

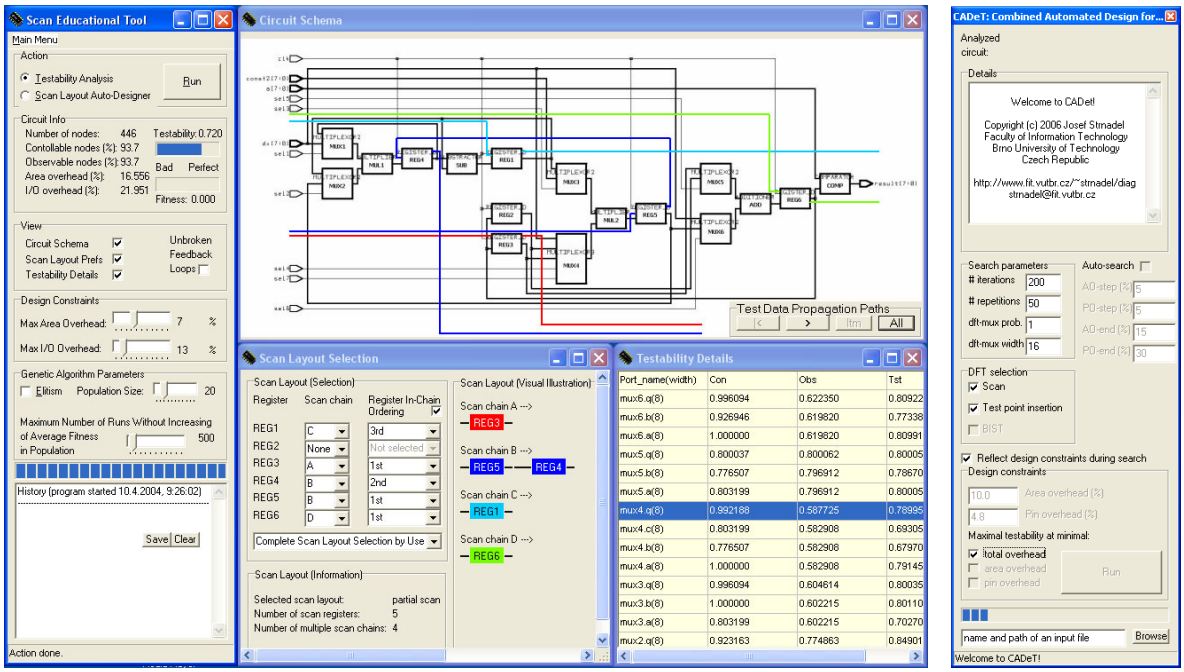


Fig. 1: Screenshots of SET tool (picture on the left) and CADeT tool (picture on the right)

In the most left window of SET tool (SET control window) depicted in Fig. 1, user can select:

- which of other SET-windows will be displayed ('*View*' part of the window),
- parameters of search-algorithm ('*Genetic Algorithm Parameters*' part),

[1] circuit property reflecting easiness of detecting/localizing physical faults in the circuit after its production
[2] one of design-for-testability techniques, which are strategies of how to design circuits to be easy testable
[3] synthesized *diffeq* benchmark circuit [2] built-in to the SET
[4] particular configuration of scan technique based on forming in-circuit registers to so-called scan-chains

- maximal price user is willing to pay for testability enhancement by means of scan technique (‘*Design Constraints*’ part of the window),
- which of TA/SA modules will be started after pressing ‘*Run*’ button (‘*Action*’ part).

Essentially, SET is able to work in two modes of operation: *TA-mode* and *design-for-testability* (*DFT*)*-mode*. In the following text, typical actions a user can do in each of the modes will be presented.

TA-mode

In TA-mode, it ca be observed how user-selected scan-layout affect diagnostic parameters of the educational circuit. This can be done by checking ‘*Scan Layout Prefs*’ check-box in SET-control window (Fig. 2). After checking the box, scan-layout selection window opens (Fig. 3).

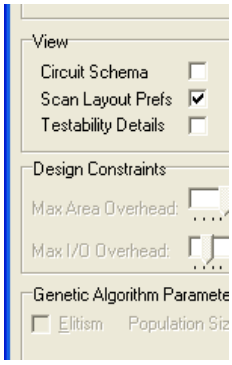


Fig. 2: Opening scan-layout widow

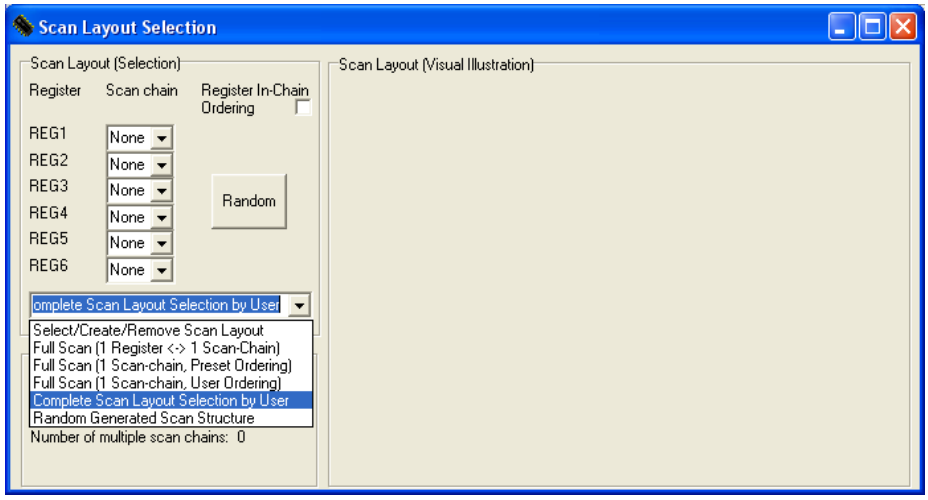


Fig. 3: Scan-layout selection widow

In the scan-layout selection window, user can select from predefined scan-layouts, choose own scan-layout, or get a random one (see Fig. 4 for illustration).

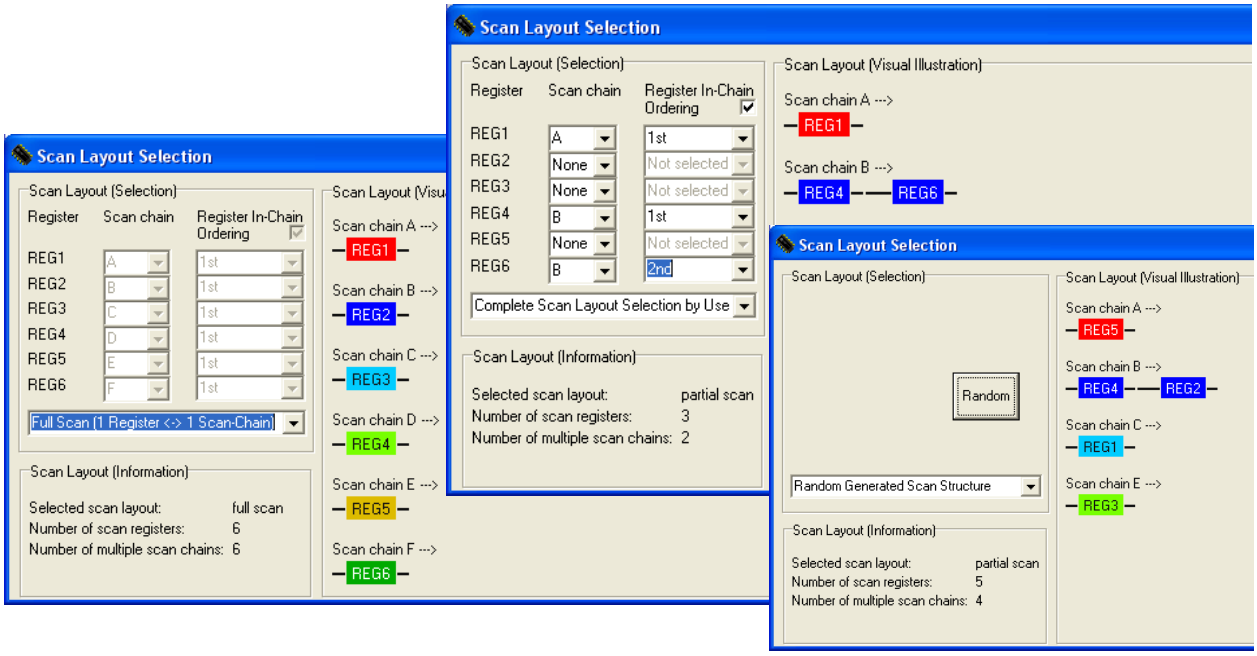


Fig. 4: Snapshots of various scan-layout selection widow configurations

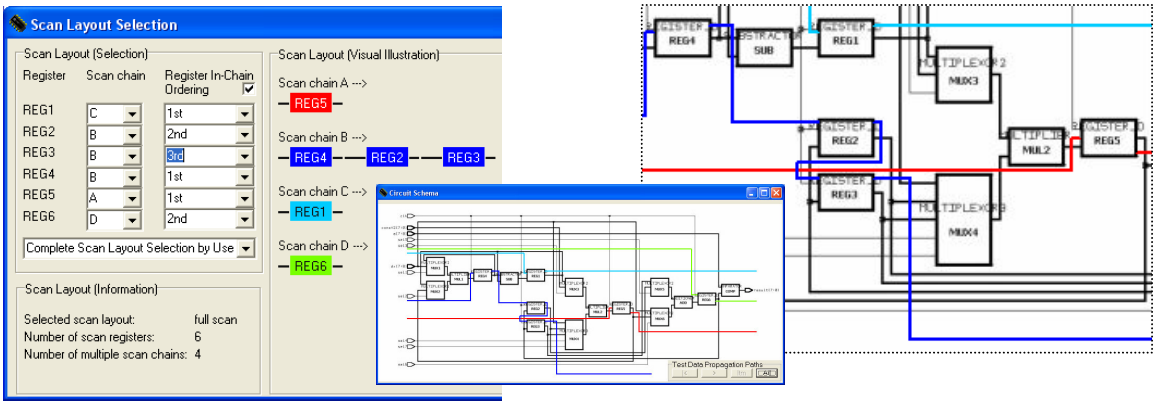
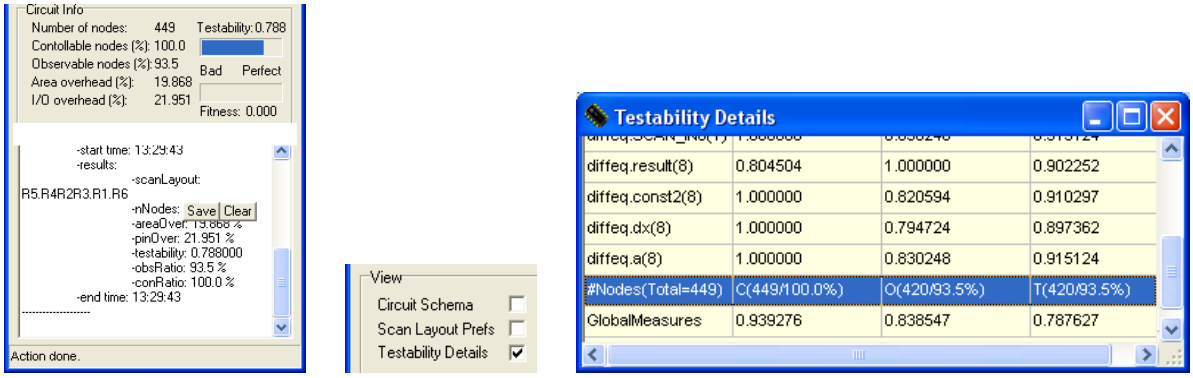


Fig. 5: Implementation of selected scan-layout (the left picture) can be visualized in 'Circuit Schema' window (the middle picture with its cutout in the right picture).

After scan-layout is selected, a user can start TA process and then observe the impact of scan-layout to circuit testability. First, '*Testability Analysis*' radio button needs to be selected. Then '*Run*' button needs to be pressed in the '*Action*' part of SET-control window. After TA process ends, testability results can be read in '*Circuit info*' and history parts of SET-control window (Fig. 6a) or (after checking '*Testability Details*' checkbox in '*View*' part – Fig. 6b), detail testability results in newly opened '*Testability Results*' window (Fig. 6c).



a) b) c)

Fig. 6: Testability analysis results according to selected scan-layout

After TA is done, user can (in '*Circuit schema*' window) observe how test-data will be propagated through the circuit structure according to selected scan-layout. Propagation process can be controlled manually by buttons in 'Test Data Propagation Paths' part of the 'Circuit schema' window and visualized in the graphical or text form (Fig. 7).

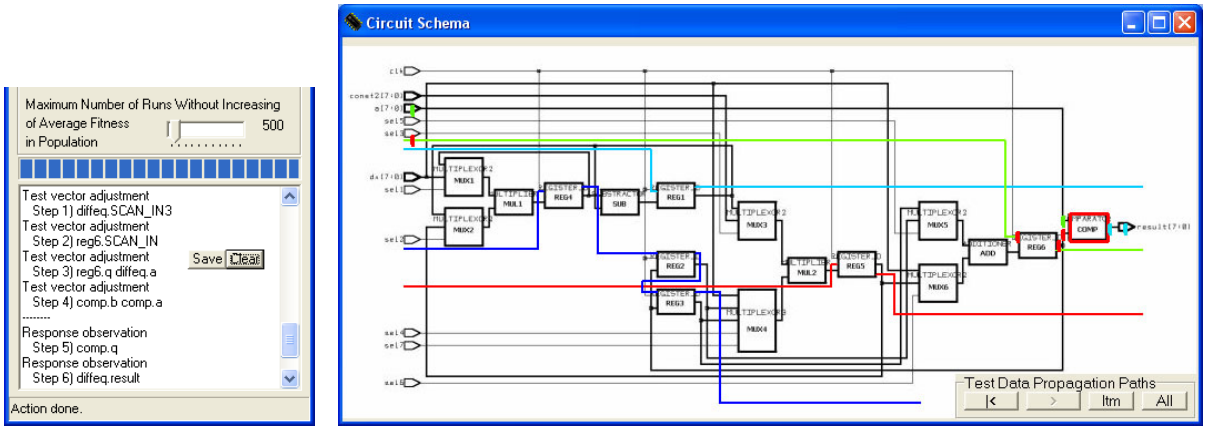


Fig. 7: Visualization of test-data propagation paths according to selected scan-layout

DFT-mode

Typical actions that can be done in DFT-mode are as follows (see Fig. 8). First, '*Scan Layout Auto Designer*' radio button is to be set in the '*Action*' part of SET-control window. Then, design constraints and search-parameters are to be set in '*Design Constraints*' and '*Genetic Algorithm Parameters*' parts. In '*Design Constraints*' part, user can specify the maximum price to be paid for testability enhancement of the circuit by means of scan technique.

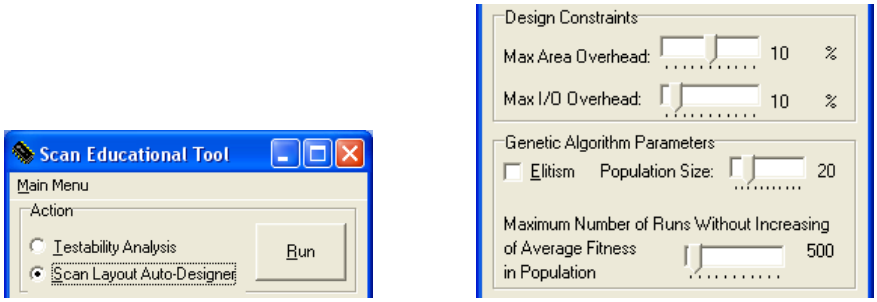


Fig. 8: Starting SA-module of SET

After '*Run*' button is pressed, SET tries to find such a scan-layout, which implementation both does not exceed user-given price and leads to significant enhancement of circuit testability. If such a solution is found under search-conditions entered in '*Genetic Algorithm Parameters*' part, it is visualized both in '*Scan Layout Selection*' and '*Circuit Schema*' windows, which are opened automatically (see, e.g., Fig. 5 for an illustration).

CADeT tool

The second tool, *CADeT* (*Combined Automated Design for testability Tool*) takes a netlist containing information about original user-given circuit structure as an input. In Fig. 9, an example of the netlist and corresponding schema for simple circuit is presented.

```
// Circuit data
CIR nested_loops In(in,8) clk(clk,1) Out(out,8)
// In-circuit modules data
ITM FU1(ADD) a(in,8) b(in,8) q(out,8)
ITM FU2(ADD) a(in,8) b(in,8) q(out,8)
ITM FU3(ADD) a(in,8) b(in,8) q(out,8)
ITM R1(REG) d(in,8) clk(clk,1) q(out,8)
ITM R2(REG) d(in,8) clk(clk,1) q(out,8)
ITM R3(REG) d(in,8) clk(clk,1) q(out,8)
// In-circuit links data
LINK nested_loops.In -> FU1.a
LINK nested_loops.clk -> R1.clk
LINK nested_loops.clk -> R2.clk
LINK nested_loops.clk -> R3.clk
LINK FU1.q -> R1.d
LINK R1.q -> FU2.a
LINK FU2.q -> R2.d
LINK R2.q -> FU3.a
LINK FU3.q -> R3.d
LINK R3.q -> FU1.b FU2.b FU3.b nested_loops.Out
```

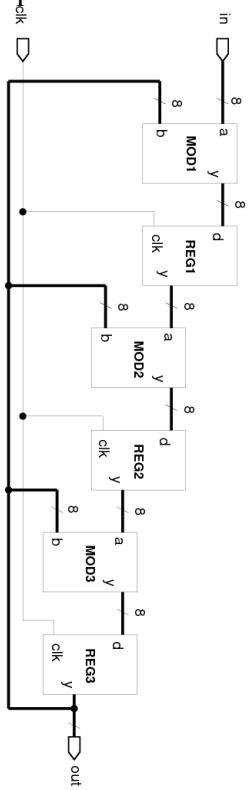


Fig. 9: nested_loops circuit – netlist (on the left) and schema (on the right)

While SET works with a fixed educational circuit and a scan technique, both built-in to the application, CADeT is able to process any circuit (i.e. from [3] benchmark suite) and utilize more DFT techniques than SET. For user-given combination of DFT-techniques, design-constraints and search parameters, CADeT explores search-space of all possible DFT-solutions and tries to find those with an acceptable cost/quality trade-off between achieved diagnostic parameters and their price in the form of meeting user-given design constraints.

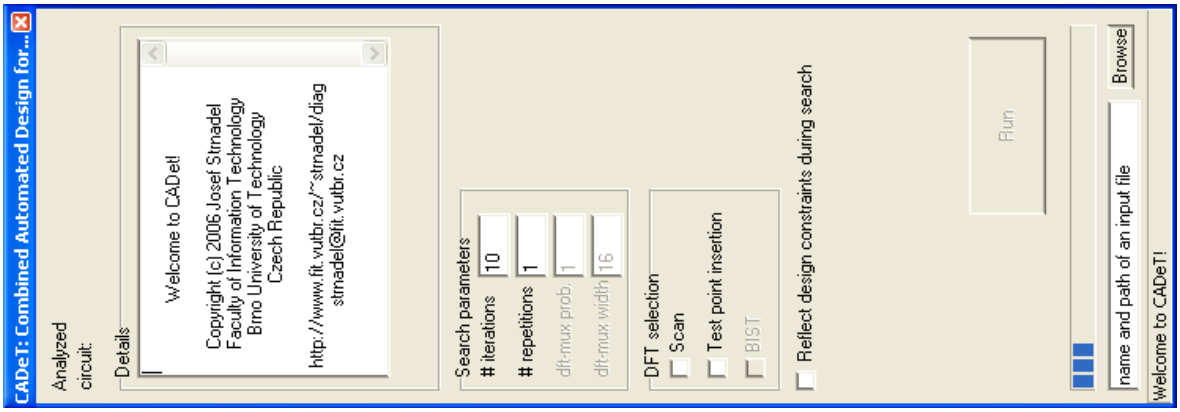


Fig. 10: CADeT - main window

Following text presents typical actions, which can be done by CADeT in order to setup and start user-desired DFT-experiments over input circuit. First of all, it is necessary to choose an input circuit. This can be done at the bottom part of CADeT's main window. Afterwards, DFT techniques to be utilized for testability enhancements are to be selected by a user (actually, one of scan, test-point-insertion[5], BIST[6] techniques or their combination can be selected). Afterwards, search-parameters like number of iterations per one experiment, number of experiment repetitions, probability-values etc. need to be set (see Fig. 11).

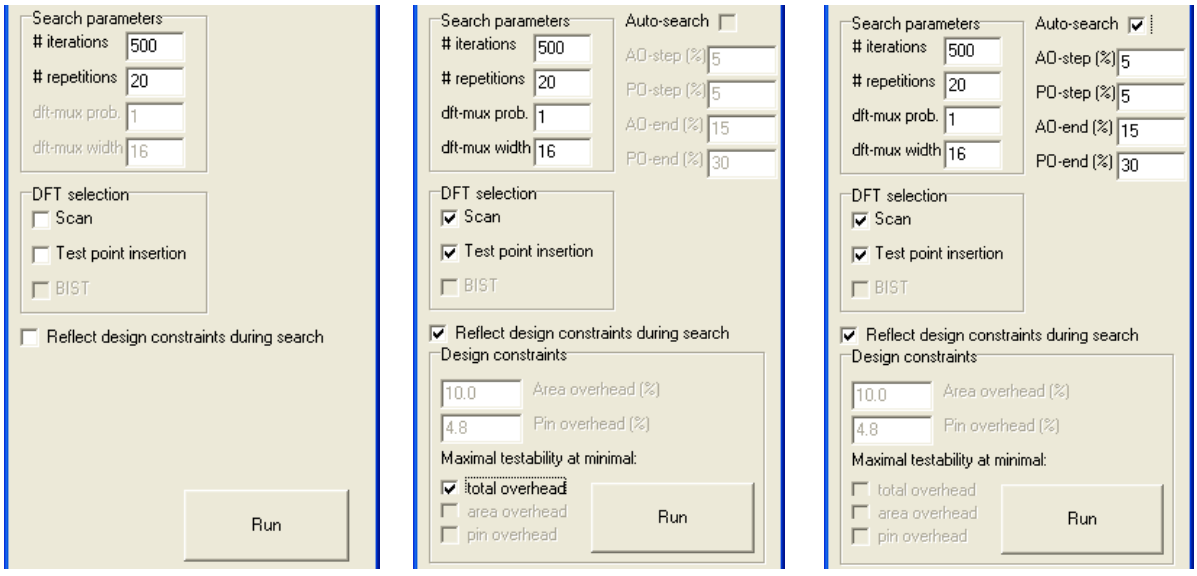


Fig. 11: Selecting search-parameters, DFT techniques and design constraints

In design-constraints related part, it is possible to set-up maximum *price* user is willing to pay (actually, in area and pin overhead parameters only) for testability enhancement of the circuit by means of selected techniques. Price can be entered directly in numeral form, or (alternatively) it is possible check one of '*total overhead*', '*area overhead*' or '*pin overhead*'

[5] DFT technique based on inserting extra logic into a circuit structure in order to make the circuit more testable
[6] abbreviation of Built-In Self Test (automated test generated by a special circuitry involved in the circuit itself)

checkboxes. If price is entered in numeral form, solutions not exceeding the price (i.e., local optimum solutions) will be searched. Otherwise, solutions with minimal total, area or pin prices (i.e., global optimum solutions) will be searched. In some cases it is needed to search solutions in certain price-range; for the purpose, it is possible to set-up the range in the ‚*Auto-search*' part and run such a kind of experiment automatically.

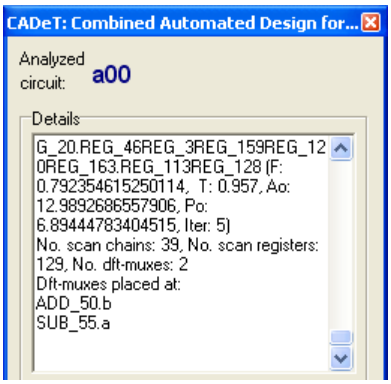


Fig. 12: Illustration to CADeT output (best solution found) for a00 circuit from [3]

After all parameters are set and '*Run*' button is pressed, CADeT tries to find out solutions having maximal testability and not exceeding user-given price. Detail information about evolution of the search-process is logged-in to text files, as well as written (in shortened form) to the '*Details*' part in the main window (see Fig. 12). Last-written solution is the best one.

Conclusion

SET and CADeT tools presented above can be utilized both in education and research areas related to diagnosis of digital systems. While SET tool is limited only to one (scan) DFT technique and one built-in educational circuit, CADeT is able to perform more sophisticated experiments with more DFT techniques and any digital circuit. Both SET and CADeT run as WIN32 applications able to store results in several file-formats (e.g., plain text, LaTEX, HTML) to be easily presented in most frequently used publishing systems. Actually, only SET part of the toolset can be freely downloaded from [4] and utilized for non-commercial purposes. CADeT will be available for downloading after it will be redesigned from work-version to public-version.

Acknowledgement

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