The Use of Genetic Algorithm to Derive Correlation Between Test Vector and Scan Register Sequences and Reduce Power Consumption

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Abstract—**In most of existing approaches, the reorganization of test vector sequence and reordering scan chains registers to reduce power consumption are solved separately, they are seen as independent procedures. In the paper it is shown that a correlation between these two processes and strong reasons to combine them into one procedure run concurrently exist. Based on this idea, it is demonstrated that search spaces of both procedures can be combined together into a single search space in order to achieve better results during the optimization process. The optimization over the united search space was tested on ISCAS85, ISCAS89 and ITC99 benchmark circuits implemented by means of CMOS primitives from AMI technological libraries. Results presented in the paper show that lower power consumption can be achieved if the correlation is reflected, i.e., if the search space is united rather than divided into separate spaces. At the end of the paper, results achieved by genetic algorithm based optimization are presented, discussed and compared with results of existing methods**. *(Abstract)*

Keywords-correlation, test application, scan chain, register. test vector, reordering, power consumption, reduction, genetic algorithm, search space, CMOS, AMI, benchmark, digital circuit

I. INTRODUCTION

Modern commercial tools are able to generate high quality sets of test vectors with high degree of fault coverage which are not usually optimized to reduce power consumption. Therefore various methods were developed to optimize the sequences of test vectors to reduce switching activities during test application. In combinational circuits the responses depend only on the set of test vectors being applied, therefore it is possible to reorganize their sequence. The responses will be the same, but their sequence will be different. It means that the sequence of test vectors can be reorganized with the goal to minimize power consumption. It can be also stated that fault coverage is the same as with the original sequence of test vectors generated by test generator. In sequential circuits the situation is different due to the fact that the responses do not depend on the actually applied test vector but on those applied in previous steps as well. The test is generated by a *SATPG* (*Sequential Automated Test Pattern Generator*). If the sequence is modified in some way then completely different test is gained with different fault of coverage. If scan register chain is inserted into the component then for test generation process the component is seen as combinational and *ATPG* (*Automated Test Pattern Generator*) can be used to generate the test. Fault coverage does not depend on the sequence of test vectors. The sequence of scan registers can be reorganized to reduce power consumption. The problem of identifying the proper sequence of test vectors/scan registers belongs to the category of NP-hard problems [7], its complexity is $O(n) = n!$ where n is the number of elements the sequence of which is supposed to be optimized. To model both problems (i.e. the sequence of scan vectors and scan registers) separate graph models are often used. To solve the problem, minimal Hamilton path must be identified in the graph. After it is found, it represents the solution of the problem, i.e. the sequence of test vectors for which the power consumption during test application is minimal is identified. Many methods exit which utilize the above described approach. E.g., in [7], Hamming distance between test vectors is analyzed in order to optimize their sequence.

It could be concluded that power consumption during test application of test vectors is somehow associated with Hamming distance between test vectors. Anyway, examples can be found in which the results do not correlate. The switching activity is difficult to be evaluated if the physical implementation of the component is not known. It can be shown that a change in one bit can cause higher switching activity than a change in several other bits (more than one bit). In [5], the problem of reordering scan registers in scan chain is solved – greedy search algorithm is used for this purpose. Methods combining *BPIC* (*Best Primary Input Change time*) approaches with test vectors reordering can achieve yet higher reduction of power consumption. In [16], the method combining these two approaches is described – it uses simulated annealing to investigate state space. These methods require special approach for test application which reduces their use in commercial diagnostic tools. Typically, optimizing methods are used sequentially (e.g. the sequence of registers in scan chains is optimized first, then the same is done for the sequence of test vectors).

II. MOTIVATION FOR THE RESEARCH

After we performed the analysis of results achieved by existing optimizing methods, we concluded that dependencies exist between these two approaches – the results of applying one method will influence the results of the other one. Therefore, the following hypothesis was defined as a starting point of our research in this area: 1) high quality results cannot be achieved when these methods are used separately, 2) power consumption will be lower when these methods are combined together, especially during investigation of state spaces of possible solutions to gain reasonable reduction of power consumption during test application.

The goals of our research can be summarized in the following way:

1. to develop and implement the methodology to reduce power consumption based on concurrent optimization of the sequence of test vectors and scan registers (i.e. run in parallel),
2. to develop a library for AMI technology describing features of elements used in the design. The library will be used for test application simulation in components implemented into AMI platform,
3. to develop and implement simulation techniques for power consumption metrics (*NTC – Number of Transition Counts* [19], *WNTC – Weighted NTC* [16], *WSA - Weighted Switching Activity* [8] etc.), AMI library will be used for this purpose. The results of simulation will be used by genetic algorithm to calculate the value of fitness function reflecting the quality of particular solution,
4. to apply genetic algorithm to investigate the state space of the task. To define the principles of coding the problem into genotype, to define algorithms to transform genotype into phenotype and vice versa,
5. to verify the methodology and compare the results with other approaches.

The use of the methodology on a particular component must result in the reduction of mean power consumption value during test application. The methodology must be applicable to components containing full scan chain (consisting of one or more scan sections). For sequential components, the optimization of test vectors sequence and reordering registers in scan chain must be performed concurrently which is not possible with previously developed and implemented methods. In addition, higher precision must be achieved in evaluating the result of particular solutions compared with methods described previously, test application simulation will be used for this purpose.

In this paper we present the results of the methodology and the comparison with previously described methods. Although the method was completely developed, implemented and verified, the description of method and its implementation details are not available in details in this paper. To provide reasons for our research and justify them by experimental results is the primary goal of the paper.

The paper is organized as follows: in section III the principles of existing methodologies are described briefly. In section IV it is described how power consumption during test application can be evaluated. Section V is devoted to basic features of our methodology while in section VI results of experiments are provided and discussed.

III. Low Power Testing – the Background

A. Low Power Testing Approaches

Two approaches for low power testing exist: the first ones are directed to reducing *dynamic portion of power consumption* (*switching power*), while the second group of methodologies have a goal to reduce its *static portion* (*leakage power*). It is important to say that in older implementations, dynamic portion of power consumption was higher than the static one – e.g., in [30], it is reported that the dynamic portion of power consumption is about 90% of the total power consumption. As a consequence, in 90 nm technology [17] the dynamic portion of power consumption is only 58% of total power consumption (according to[29], 65 nm technology is seen as the technology in which the static power consumption begins to prevail over the dynamic one). It is even more evident in technologies with higher level of integration (32 nm, 25 nm) in which the static power consumption is much higher than the dynamic one [15]. Thus, to choose proper and effective optimizing procedures to decrease power consumption, the information about the target technology to which the design will be implemented, becomes significant. In the paper, the attention is paid especially to reduction of dynamic portion of power consumption.

One of criteria used to categorize methods reducing power consumption is based on the features of test set developed to test the component under design. In this way, *Test Set Dependent* (*TSD*) and *Test Set Independent* (*TSI*) methods can be distinguished. TSD based methods use both test and circuit structure modifications, while TSI based methods use only circuit structure modification and the power reduction is independent of the test set used.

Except of TSI methods, e.g., [5][14][22], many TSD methods exist: special ATPG used to increase correlation between test vectors was presented in [31], method based on replacing don't care bits in test vectors by 1s or 0s in order to reduce switching activity [10]. Other TSD methods suggest solutions of power consumption for scan based structures. In [20], it is demonstrated how the sequence of test vectors can be transformed to avoid maximum power consumption to be exceeded. To reduce power consumption, more scan chains can be used during test application [21]. Power consumption can be also influenced by the phase at which test vectors are applied to primary inputs of the component under test. Two basic strategies exist: *ASAP* (*As Soon As Possible*) - test vectors are applied to primary inputs as soon as possible and *ALAP* (*As Late As Possible*) - test vectors are applied to primary inputs as late as possible. In [16] an algorithm calculating the most convenient istants for applying test vectors to primary inputs is described. It was demonstrated on examples that 90 – 95 % reduction to values gained by ASAP/ALAP strategies can be achieved. Within the TSD methods, so-called power-constrained test scheduling methods can be identified [23][24][25]. They are typically applied at SoC abstraction level. On this level, functional blocks or IP cores can be identified. The goals of these approaches can be summarized in the following way: a) effective utilization of all sources (connections, buses, scan chains), b) reduction of test application time, c) keeping power consumption under the highest permitted value. Because the problem of test scheduling was found to be an NP hard problem [5], various simplifying or heuristic approaches are used, e.g., [6][11][13]

typically operating over a graph representation of a problem, e.g., by means of a *TCG* (*Test Compatibility Graph*) or a *TACG* (*Test Application Conflict Graph*) [4][27].

B. Power Consumption Evaluation

It is evident that direct measuring of voltage and current delivered to a device is certainly the most precise and reliable evaluation of a power consumption during test application. The approach is rather difficult to be applied especially in implementations operating on high frequencies near technological limits. Analog measuring devices are not convenient for these purposes due to subsequent difficult processing. Digital devices must be able to sample the measured values with higher frequency compared with the operating frequency of devices under measuring. Measuring devices satisfying the requirements are very expensive and for some situations they cannot be even constructed. Sometimes it is required to identify power consumption of internal components. In these situations the direct measurement is impossible. To avoid this, indirect methods can be used which are based, e.g., on measuring temperature during test application [1] or various statistical and simulation methods can be used to evaluate power consumption. These procedures usually use some simplifying metrics.

To compare the quality of solutions aiming at reducing power consumption, NTC appears to be an applicable metric. For better comparison of solutions, other metrics can be used (e.g., WNTC, WSA). To gain the highest possible precision during simulation, it is necessary to work with the immediate value of power consumption which is computationally complex problem [18]. Statistic based methods for power consumption specification indicate low computational complexity (high speed) but the lowest precision [9]. These methods typically work with such data as the type and the number of elements in the component, average fan-out in the component, the length of scan register, etc. In [18], the following simulation methods are distinguished: methods utilizing full synthesis (simulation on physical level), methods utilizing limited synthesis and so called black boxes method. In the first group of simulation methods, the simulation is performed on the level of chip physical layout. The simulation is the most precise method but the most time consuming one. In the second group of methods, the design is mapped to the predefined set of elements (so called technological library). From models in the library simulation data with required accuracy needed for simulation can be gained. These models are developed by means of simulation on physical level and results possibly verified by measuring. The black boxes method is based on grouping selected components into blocks (black boxes). On these blocks, the responses on predefined input data are gained. During simulation the responses to input data are gained through extrapolation/interpolation from responses gained in previous step.

The criterion to compare the result of various approaches can be defined in the following way: Let: 1) P_1 be mean power consumption value during test application before applying power optimizing procedure, 2) P_2 be the mean value after applying an optimizing procedure, 3) t_1 be test application time before applying power an optimizing procedure, 4) t_2 be test application time after employing an optimizing procedure. Then, the methods satisfying the condition $P_1 \times t_1 > P_2 \times t_2$ allow to reduce power consumption during test application. It results in extension of operation time of batteries supplying power to device under test and saving energy. In literature, these methods are not explicitly distinguished by their principle. Many optimizing methods are based on iteration principle in which in every step the quality of partial solution must be verified. Therefore, a precise comparison of optimizing procedures must be involved into these approaches. It is also important to develop methods which allow to calculate power consumption during test application.

IV. Principles of the Methodology

For the purposes of the methodology, formal model was developed. It is based on theory of sets. The model reflects *structural* (primary interface of *CUA – Circuit Under Analysis*, elements in CUA, the ports of these elements, connections existing in CUA), *diagnostic* (topology of scan chains, the list of test vectors and the sequence of applying) and *electric* (switching model, power consumption during switching) properties of CUA. Algorithms were developed, they operate on the formal model.

A. Flow Diagram of the Methodology

In Figure 1, the complete flow diagram of the methodology is shown. Rhomboids indicate data which are delivered into the optimization process while rectangles demonstrate the steps of the procedure with component under analysis specification in HDL as the input into it. HDL specification is mapped into AMI technological library. Full scan chain is then configured into the design (it can be possibly split into several scan chains), DFTAdvisor is used for this purpose and the sequence of test vectors is generated by FlexTest from Mentor Graphics. All these steps belong to initialization phase of the methodology. The set of test vectors is converted into ASCII file, the VHDL or Verilog description of the component is converted into binary format. It is easier to work with these types of data than with VHDL/Verilog formats. During initializing phase, the starting population of entities is developed – consisting of the sequence of test vectors and the order of scan registers, they are then solved as a unified problem. A predefined condition (number of iterations) is determined before the optimizing procedure is started. It is also defined which solutions will be seen as satisfactory ones (in terms of power dissipation during test application). The optimizing procedure is terminated either when the predefined number of iterations is reached or the value of power consumption achieved. In each step, population entities are assessed. The assessment lies in decoding genome into the vector of priorities which determines the sequence of applying test vectors and the organization of scan chain/chains. The vectors of priorities are utilized in the simulation of test application. The simulation is performed on technological library. As a result of the simulation, a value in a selected metrics (for example NTC metric) is gained which reflects

power dissipation during test application. This value is then converted to fitness value which reflects the quality of the solution. The best solutions are then identified, the crossover and mutation of these solutions is then performed. In this way a new generation of entities (solutions) is produced. In genetic algorithms elitism is used so that the best solutions are not lost during population development. As soon as the termination condition is reached, the best entity is identified, its genome is decoded, the sequence of applying test vectors and the organization of scan chain/chains is derived which is the output of the methodology. The steps of the optimizing procedures can be recognized in dashed line area.

For the communication with the software tool user-friendly interface was developed. The user chooses one of possible dissipation metrics which will be quantified during simulation, sets parameters for genetic algorithm, and identifies both input files: the file describing the component and the file containing test set. If the test set is recognized to be incompatible, the application converts it to a compatible version first. The reorganized sequence of test vectors together with the new (i.e. optimized) sequence of scan registers are the outputs of the application. A user is also provided with the information how the values of power dissipation metrics were improved (their values before and after the optimization).

B. Problem Encoding Details

As already mentioned, genetic algorithm was used to find the solution of the problem defined in this paper. In each step, candidate solutions are recognized (*phenotypes*) and encoded into *genotypes* which carry genetic information. Genetic operators are applied on genotypes. All solutions must satisfy required quality. Therefore, principles of evaluating quality of individual solutions must be defined.

The quality evaluation is performed in several steps. First, the *genotype* is transformed into *phenotype*. The quality of particular phenotype is reflected by a real number, special function is defined for this purpose. The principle of problem encoding allows to encode both partial problems (the sequence of test vectors and scan registers order) into one structure. The structure is scalable and can encode this information for several CUAs or for CUAs containing several scan chains. This principle was used in the methodology the goal of which is the identification of testable blocks in CUA [28].

The principles of encoding are based on the existence of *chromosome CH* = (b_{i1}, b_{i2}, …… ,b_{in}) divided into *blocks* where each block reflects the sequence of test vectors or the order of scan scan chains The division is determined by information stored in *K* parameter, which is an ordered sequence of *n-1* indexes (k_1, k_2, …, k_{n-1}) used to identify bounds of *n* particular blocks within CH. The total number of blocks (*n*) is equal to the number of CUAs plus the number of scan chains. Each block consists of one or more *genes*.

In Figure 2, the structure of a double block is shown, it reflects three test vectors and three scan registers within a CUA. The first block (Block1) containing code sequences b_{i1}, b_{i2}, b_{i3} determines sequences of test vectors while in the other block (Block2) containing b_{i4}, b_{i5}, b_{i6} the sequence of scan registers in scan chain is encoded.

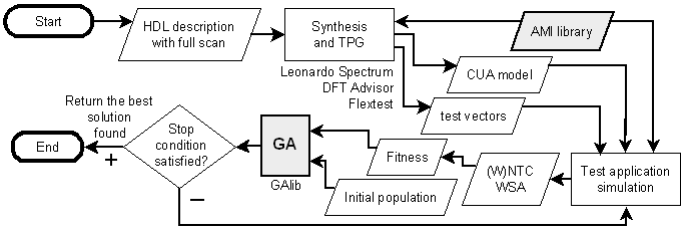

Figure 1. Flow diagram of the methodology

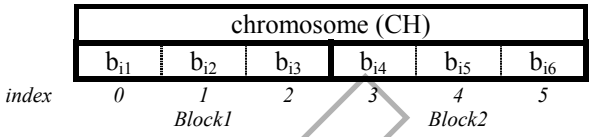

Figure 2. An Illustration to a Double Block Chromosome for K=(3). I.e., the 2nd block starts at index 3, which implies the 1st one ends at index 3-1=2.

As another example, take CH = (12, 2, 8, 10, 20, 11, 5, 9) with K=(3, 6), i.e., composed of 3 blocks (see Figure 3):

- Block1 starts at index 0 and ends at 2 of CH. In (12, 2, 8), it encodes an application sequence of 2-0+1=3 test vectors (v_1, v_2, v_3). Next blocks describe a way in which registers are organized within scan chains:
- Block2 starts at 3 and ends at 5 of CH. In (10, 20, 11), it encodes organization of 5-3+1=3 registers in the first scan chain ($sc_{1,1}$, $sc_{1,2}$, $sc_{1,3}$).
- Block3 starts at 6 and ends at 7 (i.e., *length*(CH)-1) of CH. In (5, 9), it encodes organization of 7-6+1=2 registers in the second scan chain ($sc_{2,1}$, $sc_{2,2}$).

Because the smallest value in the Block1 equals 2 (placed at index 1 of the block), then vector $v_{1+1}=v_2$ will be applied as the first one. The next higher number within the block is 8 (placed at index 2). So, vector $v_{2+1}=v_3$ will be applied as the next. 12 is the highest number within the block. It is placed at index 0, so $v_{0+1}=v_1$ will be applied as the last one. Alike, information about scan chains is extracted from CH: the 1st scan chain is ($sc_{1,1}$, $sc_{1,3}$, $sc_{1,2}$), the 2nd is ($sc_{2,1}$, $sc_{2,2}$).

On the presented chromosome structure, operators typically used in genetic algorithms like crossover and mutation are applied in each generation of solutions.

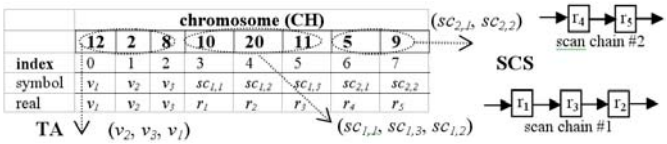

Figure 3. An Illustration to a 3-Block Chromosome

Each generation is evaluated by means of fitness function which allows to identify the best solutions to be used in the next generation of solutions. It is possible to limit the number of generations and gain satisfying solutions in acceptable times.

TABLE I. Relation between optimization type and search space size – Illistration for b15 circuit from ITC99 Set

Optimization of	Search space size		
	General formula	b15 values	
		Substituted	Enumerated
Test vector reordering	|SC|!	416!	1.44×10^{3476}
Scan chains reordering	|SC|!	416!	3.84×10^{910}
Both reorderings in sequence	|TVS|! × |SC|!	1297! × 416!	$\approx 1.44 \times 10^{3476}$
Both reorderings in parallel	|TVS|! × |SC|!	1297! × 416!	5.54×10^{4386}

Before the development and implementation of the methodology was started, the complexity of the problem was studied first. It is a well known fact that exhaustive investigation of the search space always leads to the best (optimal) solution of the problem. However, if the problem is of high complexity, it is impossible to investigate all possible solutions of the problem. The results of our investigations are summarized in TABLE I.

In the table, search space size analysis is summarized and evaluated for various optimizations performed on *b15* circuit from ITC99 benchmark set. In the first column, the type of optimization is identified. The symbols in the table have the following meaning: *TVS* is the set of test vectors, *SC* is the set of registers which can be possibly included into scan chains. In the second column, the formulas used to calculate the complexity are provided, while in the remaining columns the results for b15 circuit are provided.

Based on the analysis, it was clear that the combined problem of concurrent test set vector and scan chain reordering is a problem of high complexity which does not certainly allow to use a greedy algorithm to find the best solutions. It was decided to use optimizing procedures in the methodology.

It is important to say that these solutions are based on identifying such solutions which satisfy the required conditions reflected by a fitness function. It cannot be guaranteed that the solutions identified are optimal, they are seen as suboptimal but still satisfying required conditions.

V. Experimental Results

The main goal of the proposed method as well as of experiments performed was to compare results produced by a sequential optimization with results produced by our methodology based on parallel optimization of the solved problems. During the run of the sequential optimization, test vector sequence was optimized first before reordering registers within scan chains. Thus, two search spaces had to be explored sequentially during the optimization in previously published approaches while only one common search space is to be explored during parallel optimization of both test vector sequence and scan chains reordering.

A. Power Consumption Reduction: The Definition Utilized

Before the experimental results will be presented, it should be noted that in our approach, the power consumption reduction (r) was defined as follows:

$$r = \frac{pwr_{reduced}}{pwr_{orig}} \times 100 \quad (1)$$

where pwr_{orig} is the original power consumption of the CUA (i.e., the value before the reduction) and $pwr_{reduced}$ is the power consumption achieved after the method for reduction was applied. This implies that if r was defined in a different way from (1) in another approach (let the reduction defined the other way be denoted by r^*) – typically, using the formula

$$r^* = \left(1 - \frac{pwr_{reduced}}{pwr_{orig}}\right) \times 100 = 100 - r \quad (2)$$

it had to be re-evaluated first from r^* to r before the power consumption reduction values are compared. Here, the re-evaluation is quite simple, because it holds $r=100 - r^*$.

B. Comparison of Sequential and Parallel Optimizations

The very first experiment was run on a computational system equipped with two AMD Opteron 2220 dual core CPUs operating at 2.8 GHz. Results of both sequential and parallel optimizations performed over a subset of circuits from ISCAS89 benchmark set are presented in TABLE II. Results related to serial optimization in which ordering of registers within scan chains was optimized before test vector sequence was optimized are not available in the table because they are similar to results related to the second alternative of serial optimization during which test vector sequence was optimized before reordering registers within scan chains, the results are provided in the table.

The meaning of symbols in the table is as follows: circuit name (*circuit* column), reduction achieved if just test vector sequence was optimized (r_{vec}), reduction achieved if test vector sequence ordering and ordering of registers in scan chains were optimized sequentially (r_{sec}), time needed to perform the sequential optimization (t_{sec}), reduction achieved if both the optimizations were performed concurrently/in parallel (r_{par}) and time needed to perform the parallel optimization (t_{par}).

TABLE II. Comparison of sequential and parallel optimizations for selected ISCAS89 circuits

Circuit	r_{vec} [%]	r_{sec} [%]	t_{sec} [s]	r_{par} [%]	t_{par} [s]
s27	77.7	77.7	4.009	66.8	2.445
s298	82.1	82.1	1783.265	75.0	913.891
s344	89.0	86.7	1462.634	83.7	713.631
s349	78.1	75.7	1261.496	71.0	618.781
s382	85.1	82.4	4729.337	73.3	2492.118
s386	81.7	78.4	4748.800	70.8	2397.434
s444	80.2	76.4	4505.608	64.6	2322.130

TABLE III. The comparison of results gained by proposed metod with results presented in [12] for selected ISCAS85/ISCAS89 circuits

circuit	r_1 [%]	# TC	FC [%]	r_{2HD} [%]	r_{2NTC} [%]
c432	69.0	81	98.64	**59.9**	64.8
c880	80.0	95	100.00	**75.1**	75.0
c1355	84.4	69	99.80	**68.0**	80.0
c1908	65.7	8	42.47	**63.7**	76.1
c2670	90.1	59	59.22	**88.6**	86.4
c7552	91.5	332	99.87	**91.1**	91.2
s298	58.2	50	96.87	79.7	81.4
s444	68.9	65	97.07	73.5	64.6
s641	77.0	88	99.13	79.9	65.9
s1423	84.7	133	99.52	**82.3**	74.8
s1488	58.7	156	88.50	72.5	70.6
s5378	90.3	309	99.16	**89.0**	85.3

It is evident that better results (i.e., those with lower numeric values of *r* parameter) were gained if concurrent optimization was used. The results achieved with concurrent optimization are of a higher quality than those produced by sequential optimizations. Thus, it was indicated that our hypothesis is valid.

It was also recognized that concurrent optimization is able to produce results in shorter times than sequential optimizations. The above-mentioned observations motivated us to make further experiments allowing us to study the impact of the correlation on the quality of produced results.

C. *Results Achieved Over the Benchmark Circuits*

To verify the validity of our hypothesis, our method was applied to circuits from ISCAS85, ISCAS89 and ITC99 benchmark sets. In our methodology, the circuits were mapped onto AMI 0.5um library by means of Leonardo Spectrum tool. For combinational circuits, test vector set is the only input to the optimizing procedure, while for sequential circuits the structure of scan chain is taken into account as well. In our methodology the circuits are modified to their full scan versions by DFTAdvisor tool. The circuits contain just one scan chain. Then, both test vector sequence and reordering of registers within scan chain were optimized concurrently. Test vectors under the stack-at-fault model were generated by Flextest tool. In TABLE III. results achieved by the proposed method are compared with results produced by the method published in [12]. As a common comparison base, selected circuits from ISCAS85 and ISCAS89 benchmark sets were used. In the table, the symbols have the following meaning:

- r_1 – reduction according to results available in [12],
- *# TC* – number of test cycles needed for the circuit (in each test cycle, one test vector is applied),
- *FC* – fault coverage,
- r_{2HD} – reduction achieved by means of evaluation of Hamming distance between test vectors,
- r_{2NTC} – reduction achieved by means of NTC metric.

Results produced by our method are better than those presented in r_1 column, they are visualized in boldface.

TABLE IV. COMPARISON OF THE PROPOSED METHOD WITH THE METHOD PRESENTED IN [10], FOR SUBSET OF ISCAS85/ITC99 CIRCUITS

cir	c880	c1355	b12	c1908	c3540	c5315	c6288	c7552
r_1 [%]	89.7	85.9	61.4	78.3	82.2	90.9	91.8	68.7
r_2 [%]	**75.0**	**80.0**	**58.0**	**75.1**	**81.3**	**90.1**	**91.0**	91.2

For *c1908* combinational circuit, fault coverage achieved is only 42.47 %; the increase of the parameter would be possible after proper application of test point insertion technique. Alike, for *c2670* circuit fault coverage was 59.22 %. For other circuits, fault coverage was higher than 80 %.

The method published in [12] is based on evaluating Hamming distance between test vectors, it optimizes test vector sequence before reordering scan registers included into scan chain. In the method, problem being solved is converted to the Travelling Salesman Problem, which is solved by a genetic algorithm.

In TABLE IV. , the results achieved by the method presented in the paper are compared with those presented in [10]. The meaning of symbols in the table (and all successive ones) is the same as in previous table, i.e. r_1 represents reduction gained by other approaches while r_2 represents reduction gained by our approach. In the table, it can be recognized that (except of the results gained for *c7552* circuit) the results achieved by the proposed method represent better (i.e. numerically smaller) power reduction values. Benefits typical for parallel optimization of both test vector sequence and reordering registers in scan chains could be applicable only in *b12* circuit case because it was the only sequential circuit from ISCAS85/ITC99 benchmarks involved in the experiment. In the table, it is seen that the best result was achieved for *c880* circuit (the lowest r_2/r_1 ratio) while the worst result was achieved for *c7552* circuit (the highest r_2/r_1 ratio).

In TABLE V. , results achieved by proposed method are compared with results presented in [5]. Except of *s27* circuit, better reduction values (i.e., lower numeric values of *r*) were gained by our method. We did not find the reasons for the results gained for *s27*. Because all the circuits are sequential, benefits typical for parallel optimization of both test vector sequence and reordering of registers in scan chains could be applicable to all of the circuits. It is the fact that for most of the circuits, better reduction was achieved by the method proposed in the paper than by the method published in [5].

In Figure 4, results gained for a subset of ITC99 benchmarks are presented and compared to reduction (r1) published in [2] and [3], which are denoted as method A and B in the figure. It is evident reduction got by our method is better than reduction got by the mentioned methods

TABLE V. COMPARISON OF THE PROPOSED METHOD WITH THE METHOD PRESENTED IN [5] FOR SUBSET OF ISCAS89 CIRCUITS

cir	s27	s298	s344	s349	s382	s386	s444
r_1 [%]	44.9	90.9	92.6	91.8	92.3	84.0	95.3
r_2 [%]	66.8	**75.0**	**83.7**	**71.0**	**73.3**	**70.8**	**64.6**

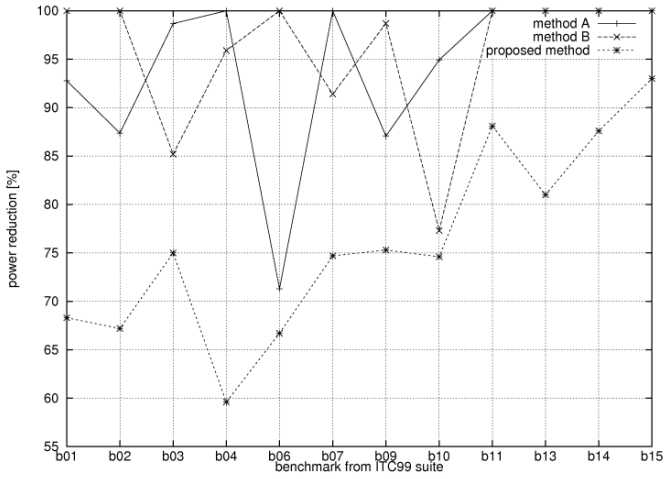

Figure 4. Results achieved over ITC99 benchmarks compared to [2][3]

VI. Scalability of the Method

In the further experiments, computational system composed of two 4-core Intel Xeon X5355 CPUs (i.e., 2x4 = 8 CPUs in total) running on 2,66 GHz was utilized. The main goal of the experiments was to test scalability of the solved task on a real multiprocessor system.

Execution times, speedups and overheads related to multiprocessor environment are visualized in Figure 5 and Figure 6. In Figure 5, execution time and speedup is visualized as a function of CPUs within multiprocessor environment, while corresponding overhead is presented in Figure 6.

Because execution times related to actions (loading of dynamic libraries, circuit verification, generation of look-up tables utilized during simulation, initial simulation etc.) are included in the overhead, it is evident that pure communication overhead will be less or equal to the presented values.

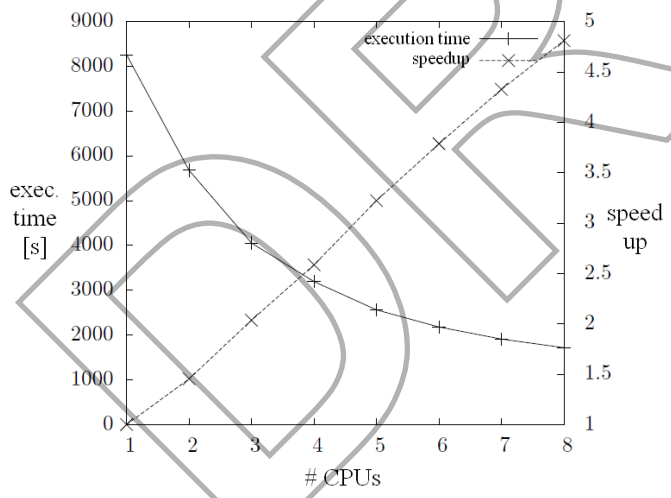

Figure 5. Speedup measured for b03

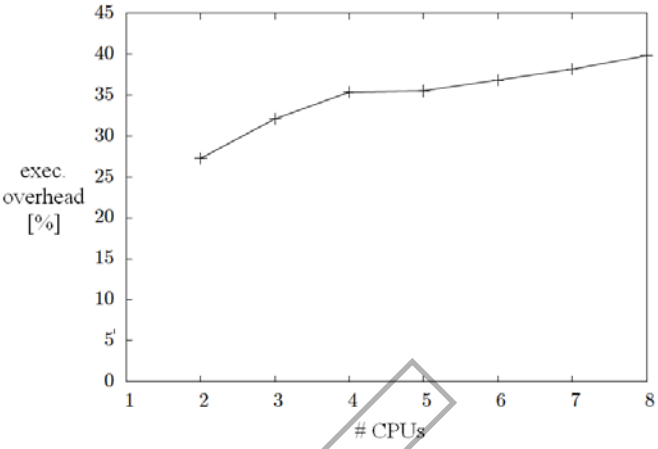

Figure 6. Parallel execution overhead for b03

VII. Conclusions

The methodology enabling the reduction of power consumption during test application was developed, implemented and verified. It is based on the hypothesis that the optimization of test vector sequence and registers in scan chain performed in parallel can bring lower values of power consumption during test application. Valuable experimental results were gained which prove the correctness of the hypothesis.

The software implementing the methodology is able to cooperate with professional tools (e.g., DFTAdvisor, Flextest and Leonardo Spectrum) and can be downloaded from [26].

The CUA was implemented into AMI platform. To evaluate the results of optimizing procedure in each step, simulation was used. The switching activity and its impact is evaluated not only on inputs of CUA but also in its internal structure which is certainly one of the advantages of the methodology. The results are then more precise compared with other methodologies, e.g. those based on Hamming distance evaluation of test vectors.

In the paper, a brief of the methodology is provided. We concentrated primarily on explaining the results of combining together two approaches which were used separately in previously published methodologies [5][10][12]. An original methodology was developed which is used on mechanisms known from genetic algorithms.

At 90 nm and below standby power consumption is a more important issue than switching activity and dynamic power consumption [15][29][30]. In our paper we offer a new trend in reducing dynamic power consumption based on reducing switching activity which can increase the importance of these methodologies.

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