Towards Implementation of Logic Circuits Based on Intrinsically Reconfigurable Organic Transistors

Vaclav Simek[1], Stanislav Stritesky[2], Michal Reznicek[3], Adam Crha[1] and Richard Ruzicka[1]
[1]Faculty of Information Technology, Brno University of Technology, Bozetechova 2, Brno, Czech Republic
[2]Faculty of Chemistry, Brno University of Technology, Purkynova 118, Brno, Czech Republic
[3]Faculty of Electrical Eng. and Comm., Brno University of Technology, Technicka 3058/10, Brno, Czech Republic
simekv@fit.vutbr.cz, xcstritesky@fch.vutbr.cz, reznicek@feec.vutbr.cz, icrha@fit.vutbr.cz, ruzicka@fit.vutbr.cz

Abstract

Nowadays, electronic circuits based on wide range of organic materials with semiconductor properties are still perceived as a somewhat unconventional design approach and fabrication technology. However, it could potentially deliver many significant advantages. Materials for organic electronics are typically lighter, flexible, easier to handle and less expensive in comparison with traditional inorganic materials used in electronics (e.g. copper and silicon used for conventional CMOS process). Previously reported research achievements in that particular domain also indicate that some of the organic semiconductor materials could be used for construction of organic field-effect transistors (OFET) that exhibit rather peculiar ability of ambipolar charge conduction. Fundamental electronic structures of such type also suggest the perspective of their utilization as the key building blocks for so called multifunctional logic elements or even more complex polymorphic circuits. In this paper, main focus is given to the introduction of organic transistor devices with the ambipolar property that would allow to further increase the efficiency of multifunctional circuit design and synthesis techniques. Important aspect depicting the novelty of the proposed approach is primarily based on the adoption of hybrid combination of the traditional silicon substrate with the deposition of suitable organic semiconductor layer. In addition, custom chip carrier platform was also developed for this purpose. Finally, the paper is concluded with review of the achieved results and suggestion of further research directions.

Introduction

Nowadays, it is possible to identify a lot of diverse application areas where a digital circuit with the inherent ability to perform a set of different functions at particular moments in time may prove to be a very efficient means of solution. Obviously the most immediate approach, how to address this specific need, is to design as many different circuits as the overall number of functions that are actually needed in a given situation. As a next step involved within the execution flow, individual outputs of these circuits are switched in such a way that only the presently required function will be taken into account. However, the main drawback behind this conception, and its essential limitation as well, will emerge in direct connection with the overall size of the resulting implementation on the circuit level that needs to be placed into a target area of a restricted dimensions.

Recent advancements within the field of digital design techniques and components for digital circuits provide a vital evidence that yet another feasible strategy may be employed – area and time-efficient circuit design based on utilization of individual structural elements exhibiting multifunctional nature [1]. In this case, the entity of multifunctional circuit is devised as a compact structure involving set of multifunctional components, where their mutual, low-level interconnection scheme remains untouched in all allowable operating modes and only the active function of these components is expected to change intentionally.

A special case related to these multifunctional circuits is based on adoption of polymorphic electronics approach [2]. Such circuits typically change their function in accordance to the actual state of a target operating environment, which is represented by a physical quantity with notable influence on some of the physical parameters of electronic structures – power supply voltage level, voltage amplitude of a signal, temperature, etc. In addition, no configuration network with a global scope or dedicated input pins of these components are required [3]. It's important to point out that change of the active function, which is executed by the polymorphic circuit, takes place immediately.

Today's applications are generally based on the exploitation of unipolar semiconductor transistors. However, the concept of polymorphic electronics has more profound nature and allows to conveniently employ new emerging devices with ambipolar behaviour. In fact, relevant aspects of the emerging materials and technologies can be approached from various standpoints through the formulation of several abstraction levels [4]. Without the ambition to provide their complete and exhaustive list, the most interesting candidates for a replacement of unipolar CMOS technology in the suggested scenario may include silicon nanowires (Si-NWs) [5, 6], carbon nanotubes [7, 8], graphene nano-ribbons [9, 10], organic polymers with semiconductor-like properties [11] and presumably even other suitable emerging nanostructures and materials [12], which make it possible to obtain new generation of advanced multi-functional logic elements.

Principles of Ambipolar Conduction

Among number of very interesting features associated with the emerging materials and nanoscale devices, especially the ambipolarity feature seems to be exposed to significant attention and, in the same time, is considered to be an important matter worth of further exploration. The actual reason or foundation might not be fully grasped in an instant manner but it obviously resides within the potential opportunity to come up with a

physical implementation of multifunctional circuits (these can be optionally referred to as reconfigurable) in a very efficient way.

From a technical point of view, fundamental principle behind the ambipolar mode of conduction is basically given by the mutual superposition of electron and hole currents. Physical devices built with this unique principle in mind offer an exceptional opportunity how to impose a direct control on electron-hole recombination taking place within the semiconductor channel. Ambipolar behaviour that can provide both n- and p-channel performance in just a single device is very important due to its tremendous importance for manufacturing of complementary integrated circuits, where it basically eliminates the need to perform micropatterning of the individual p- and n-channel semiconductors. As a direct result of that, only a single type of an elementary switching device (let's say transistor) is sufficient in comparison with conventional CMOS fabrication technology.

Some of the advanced nanoscale devices provides transparent and reliable means how to take a precise control over this behaviour and obtain significant benefits for digital-like circuits. Ambipolar mode of conduction has been already observed in many next-generation devices, e.g. comprising nanotubes, graphene, silicon nanowires, organic single crystals, and organic semiconductor structures. As opposed to the unipolar silicon MOSFET device whose p-type or n-type behaviour is unambiguously specified during fabrication, ambipolar devices can be switched from p-type to n-type, for example, by changing the gate bias intensity or drain-source polarity.

Introduction to Organic Ambipolar Transistors

Analysis of charge carrier mobility in semiconductor materials has the origins in techniques of current-voltage measurement of field effect transistors (FET). In addition, this particular property has a profound influence on the switching performance which can be achieved with such devices. General conception of field effect transistor [13] was introduced for the first time by J.E. Lilienfeld, who received a patent for his idea in 1930. William Shockley, John Bardeen and Walter Brattain developed the first physical prototype of a transistor in 1947 [14]. In 1956, these researchers were awarded Nobel Prize in physics. In 1987, Koezuka and co-workers reported the first organic field-effect transistor based on a polymeric compound which consisted of thiophene molecules [15].

The particular structural composition of a semiconductor layer can also identify several types of ambipolar transistors: bilayer, blend and single component transistors. Bilayer transistors are often fabricated via vacuum deposition because solution processed films are difficult to realize without damage to the first layer. Such transistor consists of n- and p-channel as two layer sandwich at one device. Blend ambipolar transistors strongly depend on the blend composition and the phase-separated morphology and for these reasons are highly dependent on processing conditions. Single-component OFETs have great advantages compared to the ones mentioned above. In this case, organic semiconductor (OS) layer must be suitable for both electron and hole injection and transport. Position of HOMO and LUMO level are a key factor for ambipolar transporting semiconductors. The OS is required to have a HOMO level below -5.0 eV to achieve stable hole transport and -4.0 eV for LUMO [16].

Design of Experimental Hybrid Ambipolar Devices

OFET devices were fabricated according to a bottom gate, bottom contact geometry on heavily doped Si wafers obtained from Fraunhofer IPMS [17], with a 230 nm SiO_2 layer with 30 nm Au electrodes on a 10 nm ITO adhesion layer. Two different architectures of substrates were used. First with 16 single transistors with different channel lengths (4x (2.5, 5, 10 and 20 um)) and a width of 10 mm. Second architecture was up to 36 single transistors are interconnected to inverters and ring oscillators (see Fig. 1 below).

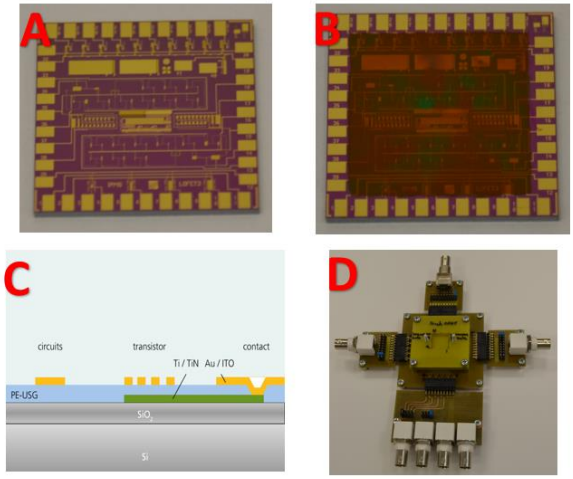

Fig. 1. View of LOFET substrate before (A) and after deposition of organic semiconductor layer (B), its layer stackup (C) and developed measurement tool (D).

The electrodes at second architecture had different channel lengths (L = 2.5, 5, 10, 20 and 40 um) and a width of 2 mm. Substrates were cleaned in an ultrasonic bath in acetone for 10 min and dried with N2, then rinsed in an ultrasonic bath with isopropyl alcohol (IPA) for 10 min and dried with N2, then cleaned for 2 min in oxygen plasma for both substrates. The PFBT SAMs were formed by immersing the silicon wafers in a 5 mM solution of anhydrous toluene for 5 min at 20 °C. After the formation of the PFBT SAMs, the substrates were rinsed with IPA and dried with N2. The octadecyltrichlorosilane (OTS) SAMs were formed by immersing the silicon wafers in a 10 mM toluene solution (anhydrous) for 10 min at 70 °C. Then the substrates were rinsed with IPA and dried with N2. The hexamethyldisilazane (HMDS) was dropped on the substrate and left there for 1 minute. Then the substrate was spun at 1000 rpm and a drop of chlorobenzene was dynamically spincoated until dried up. The preparations of all monolayers proceeded in a nitrogen glovebox for first architecture. At second architecture, the creating of monolayers can´t be used

(different dielectric layers). Organic semiconductors of Tips-Pentacene, PCBM-C60 and P3HT solution were deposited by spincoating a 15 mg/ml solution at 1500 rpm on both architecture.

Design and Fabrication of Chip Expander

In order to thoroughly examine the relevant electrical properties of the experimental transistor devices built with the ambipolar behaviour in mind, where these are exploiting the seamless hybrid integration of the organic semiconductor layer with the underlying silicon-based chip substrate structure, it is necessary to temporarily attach the input and output terminals in an easy way to the available measurement and testing instrumentation equipment. One method how to approach this task is to place the chip slice onto a specifically designed carrier board and then fan-out its terminal pads by means of wirebonding technology - thin wires (Au, AlSi) with a diameter of 17 um to 150 um (according to the needs of a given application scenario) to the available conductive tracks. Customized platform delivering exactly these features is therefore called chip expender. Its physical appearance in case of the hybrid organic devices can be seen on Fig. 2 below.

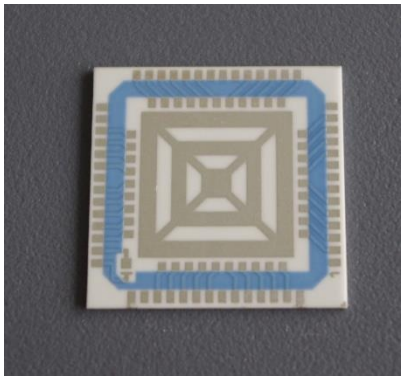

Fig. 2. Chip expander platform designed for the experimental hybrid semiconductor device [22].

Realization of Carrier Substrate

As an initial basis for the construction of the chip expander there are employed ceramic plates made of Al_2O_3 compound with a specific thickness of 0.632 mm. For the actual realization chip expander substrates with dimensions of 1" x 1" are used. These substrates are commonly used as carriers of various structures in the domain of thick film hybrid integrated circuits. As a first step preceding the actual deposition of the conductive layer it is necessary to clean the surface of these substrates by isopropyl alcohol in an ultrasonic bath, which is then followed by rinsing with deionized water. In either case it's truly vital to get rid of any impurities residing on a surface of the substrate through this particular procedure, which could otherwise cause defects and significantly impair the conductive motive.

The conductive layer is used for an easy expansion of the signals across the substrate surface and it is prepared with a silver thick-film pastes ESL 9912-K [19], which is deposited by means of screen printing technology.

Layer created in this way is reaching a thickness of about 60 microns just before the drying procedure. After the drying phase performed in an oven at 125 °C for 15 min, the layer thickness is reduced to 35 microns due to the evaporation of its volatile components. The dried structure is further cured in the oven at 850 °C with a peak at time of 10min, where the overall processing takes 1h. If desirable, it is also feasible to print the insulating layer (overglaze composition ESL 4774-BCG) [20], which is used as a solder mask in order to prevent the spillage of molten solder during subsequent mounting of the expander pins. This layer is also has to get through the curing at 125 °C for 15 minutes, but the firing profile is 525 °C with a peak at time 10 to 15min and total firing cycle of 40 min.

The external mounting leads are made by using etched stencil at 1.27 mm pitch. These leads are dimensionally etched from ALPAKA ($CuNi_{18}Zn_{20}$) material with a thickness of 150 microns. Its current carrying capacity is about 5A. Furthermore, these leads are adjusted and mechanically fixed by soldering or gluing, as required by a particular application. In order to properly address the needs in low temperature range the most commonly used choice is comprising eutectic SnPb solder alloy or more often conductive adhesive EPOTEK H31D. For high temperature applications of up to 350 °C brazing alloy $Cd_{95}Ag_5$ is used instead. Final appearance of the expander platform, as it was designed for the hybrid organic device based on LOFET substrate, can be seen on Fig. 3 below.

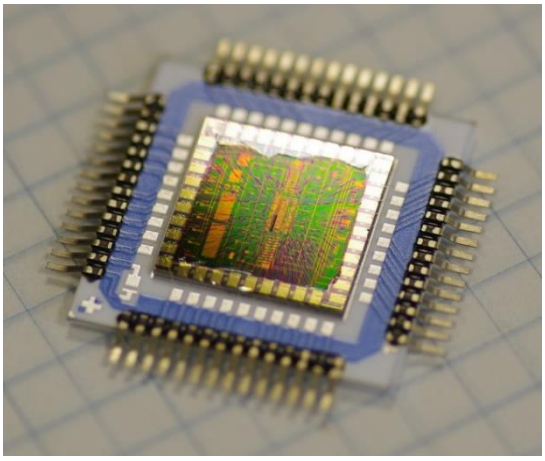

Fig. 3. Experimental hybrid semiconductor device mounted on the chip expander platform and interconnected by golden wires (wirebonding).

Attachment and Bonding of Experimental Devices

Secure attachment of the experimental chip to expander platform is achieved with the alternative application of conductive or non-conductive adhesive, according to the specific needs. If it is necessary to establish reliable conductive mating of the chip die with the expander surface, then one-component epoxy adhesive EPOTEK H31D from Epoxy Technology is used. Minimum bond line cure schedule in this case is

150 °C / 1 hour. The adhesive is applied in a form of predetermined shapes directly onto the surface of chip expander by dispenser in a quantity which ensures the achievement of about 20 to 30 microns thick layer once the chip is pressed into its corresponding location.

In case that the conductive connection is not required, it is possible to use one-component epoxy adhesive EPOTEK H61 with high thermal conductivity, whose minimum bond line cure schedule is 150 °C / 30 minutes. In the case of low temperature resistance of the chip it is possible to use alternative bond line cure schedule of 120 °C / 60 min. After drying, the adhesive operating strength range is falling into the range of -55 °C to 300 °C and is qualified even for space applications.

Glued chip die is attached to the conductive layer of the expander through the wirebonding technology [21]. This technological step is primarily using Au and AlSi wires, mostly with a diameter of roughly 25 um. Let's note that ultrasonic excitation was used during the bonding procedure in case of the fabricated experimental chip. Besides other aspects the bonding process parameters are dependent primarily on the structure of the contacted layer on the chip die and also on their current properties (oxidation, aging, etc.).

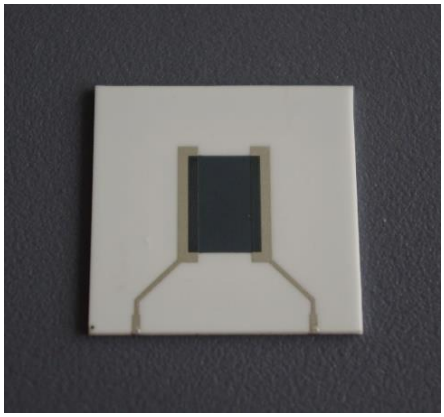

Fig. 4. Thick film heating element integrated on the reverse side of chip expander.

Heating of Chip Expander

If the application naturally requires a chip operation to be executed at a controlled temperature higher than the one available in a typical ambient environment, it is possible to equip the reverse side of chip expander with a thick film heating element, see Fig. 4 above for details in case of the fabricated chip expander platform. Thanks to the capabilities of this heating system it is possible to reach temperatures reaching the level of approximately up to 350 °C. To measure and stabilize this temperature, miniature semiconductor chip involving PN junction is deployed for exactly that purpose. Its placement can be found on the front side in the immediate vicinity of the experimental chip. This arrangement helps to establish temperature control feedback loop once combined with necessary external components.

Experimental Results and Measurements

Parameters for characterisation of OFET transistors are summarized in IEEE 1620 standard. This standard describes test methods for characterisation OFET, common sources of measurement errors and provides guidelines for extraction of measured parameters of devices. The standard provides a method for systematic characterization of organic transistors and intends to maximize reproducibility of published results by providing a framework for testing organic devices. The information describing hole mobility (μ) was extracted from the slope of the transfer curves in the saturation regime (V_{SD} = 40V) via following equation (1):

$$\mu = \frac{I_{\mathrm{SD}}}{\left(V_{\mathrm{GD}} - V_{\mathrm{T}}\right)^2} \cdot \frac{2L}{WC_i} \tag{1}$$

where L is channel length, W is channel width, C_i is capacity of dielectric, V_T is threshold voltage, I_{SD} is current between source and drain electrode at constant V_{SD} voltage and V_{GD} is gate voltage.

The field effect output characteristics were obtained during measurement performed with a dedicated probe-station equipped with Keithley 6487 picoampermeter and Keithley 617 electrometer in case of the first architecture of substrate (Fig. 5) to depict the transistor behaviour. The output and transfer characteristics plots of the second device architecture were measured in a dry nitrogen glove box with a dark enclosure shut and also at a room ambient light conditions in order to investigate the ambipolar properties (Fig. 6).

The transistors created by mixture of Tips-Pentacene showed ambipolar characteristics with relatively high threshold voltages. Calculations based on the obtained results clearly reveal the mobilities reaching the values of 2.23×10^{-3} and 0.57×10^{-3} cm2/Vs for electron and hole mobility respectively. These values are relatively high in situation when mixture of organic semiconductors was used. In this context the best mobilities were observed for Rubrene with mobility ~ 40 cm2/Vs [18].

Measurement of far more complex transistor topologies, which are also available at the LOFET substrate, can´t be conceived because of high threshold values and operating voltages falling beyond the useful range of the available lab instruments. Loss voltages also prevent to a large extent the mutual interconnection of several transistors due to the eminent difficulty to control over their on/off state. The disadvantages will be aim of our next research to achieve lower operating voltages and obtain higher values of charge carrier mobilities.

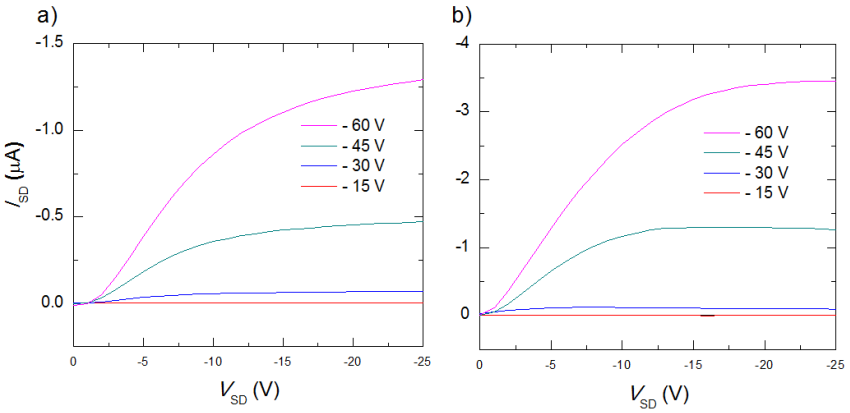

Fig. 5. The output characteristics of a) P3HT and b) Pentacene.

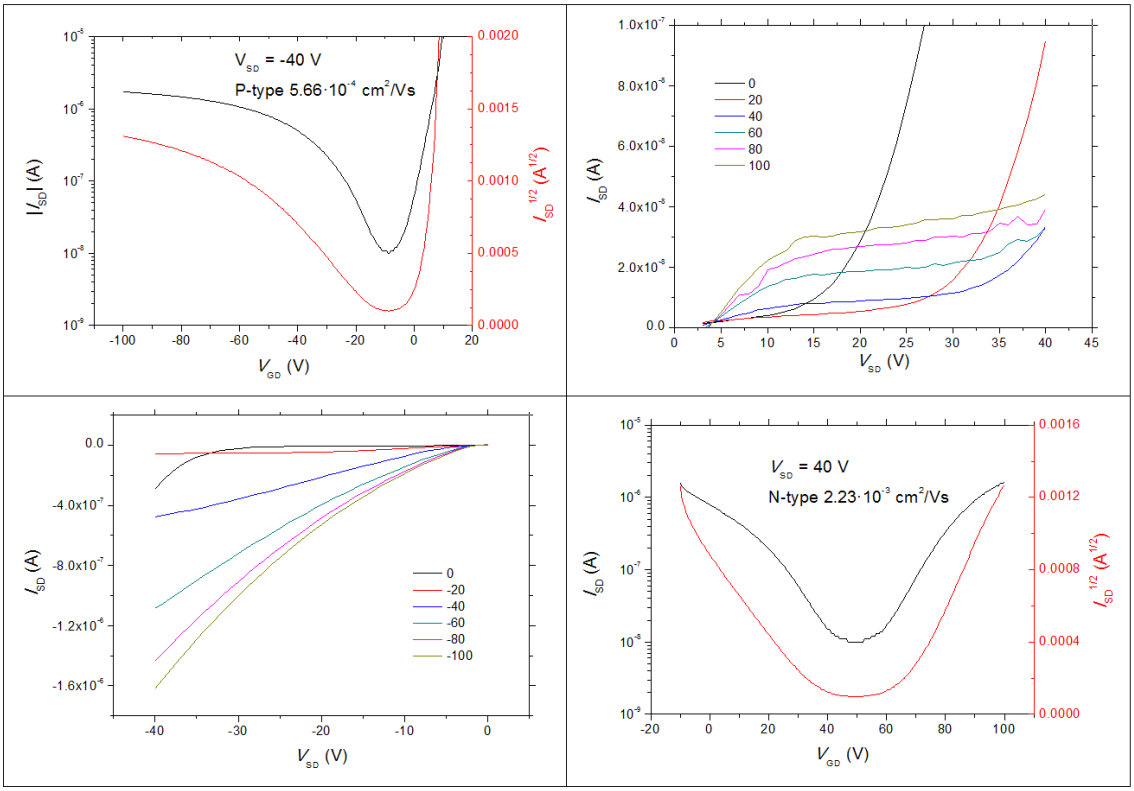

Fig. 6. The ambipolar characteristics of mixture Tips-Pentacene and PCBM-C60.

Conclusions

The objective to design and physically fabricated a couple of prototype hybrid organic-based transistors with the intrinsically built-in ambipolar mode of conduction has been successfully achieved. However, the results obtained especially during the subsequent measurement and analysis have revealed certain issues connected with the electrical properties of such devices. Especially high loss voltage observed during the mutual interconnection of several individual transistors prevented a reliable control of their on/off state. These disadvantages will be within the centre of attention during further research activities in order to achieve lower operating voltages and obtain higher values of charge carrier mobilities.

Design and fabrication of the physical transistor devices was also complemented by the proposal of custom chip carrier platform that significantly facilitates handling of the finished substrate with deposited organic layer outside the lab conditions. In addition, this particular platform makes it possible to perform also temperature-dependent evaluation of the ambipolar hybrid organic transistors.

In general, individual devices exhibited acceptable parameters in terms of charge carrier mobility, ON/OFF ratios or shapes of the measured transfer and output characteristics. Nevertheless certain modifications have to be introduced into the fabrication process in order to mitigate the aforementioned imperfections. But the feasibility of the initial theoretical concept of ambipolar conduction has been undoubtedly confirmed. It turns out that proper exploitation of ambipolar circuit components built upon the modern materials could definitely bring significant advantages for digital circuits domain.

Acknowledgments

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