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Special Section: Bio-inspired Hardware and Evolvable Systems

Guest Editorial: Bio-inspired Hardware and Evolvable Systems

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The field of bio-inspired hardware and evolvable systems poses unique challenges in the research of theories, algorithms, software, and hardware. One of the major common challenges is to translate, effectively and efficiently, mechanisms from biology into hardware. It is not just about how to implement smart algorithms in hardware, but more about how to make hardware itself smarter by making it adapt its structure and functionality autonomously in dynamic and uncertain environments. This vision of making hardware 'truly adaptive' is a huge challenge because silicon hardware is only changeable through built-in reconfiguration options. For example, capturing the full complexity of an organism in a *faithful-to-biology* model to build a fault tolerant system will inevitably result in prohibitive area overhead and reduced performance. This requires solutions that are simplified to a degree – where overhead and performance are acceptable – but which still exhibit the desired features of the biological inspiration.

Today's systems are opening up great opportunities for bio-inspired approaches since, in modern technologies, area and raw clock speed are no longer the main concerns in terms of overheads and performance. New concerns are variability, power consumption, heat dissipation and reliability, with system architectures moving towards system-on-chip, many-core, and heterogeneity. These requirements are a perfect match for bio-inspired approaches, capturing key properties of biological organisms that have evolved to be inherently energy efficient, exhibit great diversity, adapt to different environments and operating conditions, and scale effectively. This is also an opportunity because it encourages us to think about and explore other substrates that could perform computations in a more flexible and adaptable way.

This Special Section addresses these fundamental challenges when taking biological inspiration to hardware implementation. Three papers are presented which consider issues related to efficient circuit implementations of neural network elements, communication mechanisms in on-chip neural networks, and design of energy-efficient approximate circuits.

In the first paper, *Hybrid Spin-CMOS Stochastic Spiking Neuron for High-Speed Emulation of In-Vivo Neuron Dynamics*, written by Steven D. Pyle, Kerem Y. Camsar and Ronald F. DeMara, a spintronic stochastic spiking neuron was developed which shows biologically-mimetic stochastic spiking characteristics observed within in-vivo cortical neurons. This solution exhibits very fast information processing and a favourable energy profile.

The second paper, *On-chip Communication for Neuro-Glia Networks,* written by George Martin, Jim Harkin and Liam McDaid, is looking at making use of regulatory astrocytes within spiking neural networks to improve hardware fault tolerance and autonomous self-repair. Specifically, a scalable, efficient multi-layer communication network for artificial astrocytes and neurons is developed.

The final paper, *The Role of Circuit Representation in Evolutionary Design of Energy-Efficient Approximate Circuits*, written by Vojtech Mrazek, Zdenek Vasicek and Radek Hrbacek, analyses the impact of circuit representation on the quality of digital circuits produced by means of automated evolutionary algorithm-based design methodology. The case study is oriented to the area of approximate arithmetic circuits.

The contributions to this Special Section highlight the significant current challenges of making hardware systems more 'self-aware', in the sense of more power efficient, reliable and autonomously adaptive, and themselves propose a range of possible solutions.

Guest Editor Biographies

Martin A. Trefzer is Senior Lecturer (Associate Professor) in the Department of Electronic Engineering at the University of York, UK. His research interests include variability-aware analogue and digital hardware design, biologically motivated models of hardware design, evolutionary computation, and autonomous fault-tolerance. He is researching computational capabilities of CNTs, including direct evolution and reservoir computing models. His vision is to create novel architectures and autonomous systems, which are dynamically self-optimising and inherently fault-tolerant, by porting key enabling features and mechanisms from nature to hardware. He is a senior member of the IEEE, co-chair of the International Conference on Evolvable Systems (ICES), and chair of the IEEE Task Force on Evolvable Hardware.

Lukas Sekanina is a full professor and Head of the Department of Computers Systems at Faculty of Information Technology, Brno University of Technology, Czech Republic. He was awarded with the Fulbright scholarship to work with NASA Jet Propulsion Laboratory at Caltech, Pasadena, CA in 2004. He was a visiting professor with CEI UPM Madrid (2012), visiting lecturer with Pennsylvania State University (2001) and visiting researcher with University of Oslo (2001). He has served as a program committee member of evolutionary computation as well as circuit design conferences, associate editor of IEEE Transactions on Evolutionary Computation, editorial board member of Genetic Programming and Evolvable Machines Journal, International Journal of Innovative Computing and Applications, and Radioengineering. His research interests include evolutionary circuit design, evolvable hardware and approximate computing. He is a senior member of the IEEE.