Decreasing Test Time by Scan Chain Reorganization

Pavel Bartoš
Faculty of Information Technology
Brno University of Technology
Bozetechova 2, Brno,
612 66, Czech Republic
Email: ibartos@fit.vutbr.cz
www.fit.vutbr.cz/˜ibartos

Zdeněk Kotásek
Faculty of Information Technology
Brno University of Technology
Bozetechova 2, Brno,
612 66, Czech Republic
Email: kotasek@fit.vutbr.cz
www.fit.vutbr.cz/˜kotasek

Jan Dohnal
ON Design Czech s.r.o.
(On Semiconductor)
Videnska 204/125, Brno,
619 00, Czech Republic
Email: jan.dohnal@onsemi.com

***Abstract*—In this paper, methodology for scan chain optimisation performed after physical layout is presented. It is shown how the methodology can be used to decrease test time of component under test if scan chain is reorganized. The principles of the methodology are based on eliminating some types of faults in the physical layout and subsequent reduction of the number of test vectors needed to test the scan chain. As a result, component test application time is decreased. The methodology was verified on several circuits, experimental results are provided and discussed. It is expected that the results of our methodology can be used in mass production of electronic components where any reduction of test time is of great importance.**

I. Introduction

The increase of component density appearing in modern digital and analog devices requires new approaches to be used to test them, scan chain being one of these approaches. It holds that it was always very important to develop high quality tests used in the production phase. The identification of faulty components immediately after the production is certainly a cheaper procedure than their identification after it is included into an electronic device.

One possibility how to apply test to an electronic component is through its primary inputs/outputs. For complex components with high number of internal units, this approach cannot be used [1], [2]. The reason for scan-based approaches is to make internal components more controllable/observable during test application. Registers which cover certain function during operational mode are converted into serial shift registers through which test vectors/responses to them are transported, the frequency of shifting possibly becoming one of the parameters of test application effectiveness. In our opinion, the reordering of scan chain to improve test quality needs to be studied. The reordering does not change the function of the component, it holds for testability parameters as well. In the past, the reordering of scan chain was used to simplify the process of routing [3] and to reduce power dissipation during test application through the reduction of switching activity [4], [5]. The increased power dissipation of a component during test application can have serious consequences such as supply voltage drop-out, wire damage caused by electromigration, crosstalk caused by electromagnetic induction and the increase of chip temperature. Methods aiming at lowering static and dynamic power dissipation on the basis of test vectors or flip-flops reordering are known as well [6]. These methodologies have the increase of delay fault coverage as its goal as well [7].

When quality of test is evaluated, not only testability parameters but also the time needed to apply the test are important. It holds especially for tests used in the production phase of electronic component which are produced in high numbers. Even a short reduction of test application time has an impact on production costs. Faster/shorter tests can increase the number of components produced.

In our research, we deal with the idea of reducing the number of test vectors needed to verify proper function of circuit. As the input to the methodology, scan chain physical layout is used (the output of professional design system). Generally stated, we try to reduce the number of faults which can appear, thus reducing the number of test vectors to recognize these faults. It is clear that the number of test vectors reduction results in test time decrease.

The structure of the paper is as follows. First, the motivation for our research is described. Then, the basic principles of the methodology are provided. Experimental results are presented and discussed together with our intentions for future research at the end of the paper.

II. Motivation for the Research

To manufacture a mixed-signal integrated circuits a lower resolution technology is still frequently used (typically 0,25–0,7 μm). It causes that complex circuits are spacious and manufacturing costs are high. One way how to cut manufacturing costs while maintaining chip area needed for the component implementation is through the reduction of interconnecting metal layers. This does not affect the analog part of the component significantly, because there are much less wires than in the digital part [8]. Anyway, in the digital part, the following effects appear during automatic place and route procedure:

- Wires stretching – place and route tool cannot realize the shortest path.
- Rising count of vias in metal layers – place and route tool cannot realize the path in one layer.

- Realizing of long wires is difficult, because the layers are overfilled.

In some cases the place and route tool is unable to interconnect circuit parts and keep circuit area in predefined limits. Even when it is achieved, then a large number of long wires and metal vias results in lower component dependability.

We compared wires length and possible bridging faults[1] list of a few real circuits which were gained from a company doing professional designs. We found that longer wires are more susceptible to create bridging faults then shorter wires, see graph of results in the Fig. 1. Long wires also have more vias between layers, so they are more susceptible to open-wire faults.

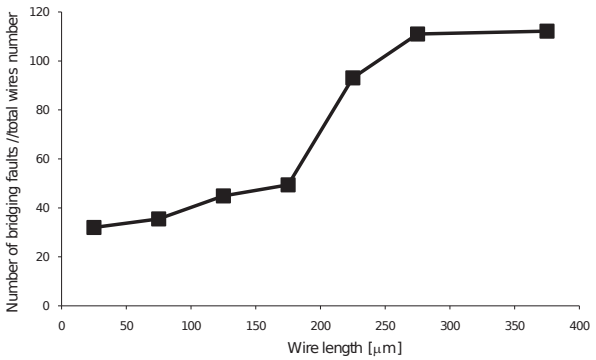

Fig. 1. Susceptibility to bridging faults dependence on wires length.

To test open-wire faults of metal vias, common test vectors for testing stuck-at faults can be used. But the testing of bridging faults requires higher number of test vectors because it is required to use each of 4 logic combinations to detect a bridging fault between a pair of wires.

The goals of our research are based on the following hypotheses:

1) in the physical layout produced by a design system it is possible to identify long wires, their number can be reduced
2) as a consequence of the reduction of long wires number, the number of test vectors to test them can be possibly decreased
3) based on the two hypotheses, we see the possibility of shortening testing phase after an electronic component is produced which can decrease production costs.

III. Description of the Methodology

During the design of a common integrated circuit, the length of wires cannot be affected. The only possibility exists during floorplanning by placing functional blocks in adjacent positions. The floorplanning is done by place and route tool, its primary goal is to keep timing constraints. To summarize, we are not able to shorten connections between functional blocks.

[1]a short-circuit between two signal lines [9]

However the interconnection of scan chain can be changed through the modification of flip-flops order. Scan chain is included to netlist after logic synthesis when the information on physical location of flip-flops is not available yet. Thus, the information about physical location of flip-flops cannot be used when the scan chain is included into the design. The inclusion is done on the level of logical structure.

In our research, we first tried to verify that after physical place and route procedure the circuit contains high number of long connections between flip-flops. For this purpose, a visualization tool was developed first which allowed us to recognize that many flip-flops are really interconnected by long connections which are routed through large chip area.

Based on the analysis of flip-flops locations, the interconnect of scan chain (order of flip-flops) can be changed in order to shorten lengths of wires. For the modified flip-flops order a re-route process is performed (without any change of flip-flops locations).

Then, the modified complete design process of an electronic component consists of the following steps (see Fig. 2):

1) logic synthesis from register transfer level (RTL) into netlist
2) physical place and route
3) modification of scan chain flip-flops order with flip-flops locations as the input
4) modification of netlist
5) new physical interconnection (re-route)

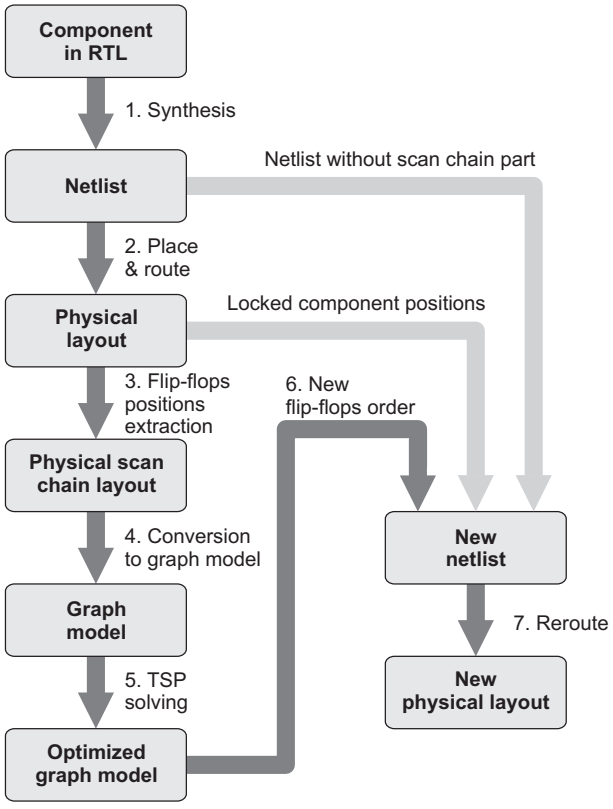

Fig. 2. Modified complete design process flow chart.

Scan chain optimization is done by reordering flip-flops in chain because modification of flip-flops locations is impossible. The goal of optimization is to minimize the length of interconnect wires between flip-flops.

The scan chain can be formalized into mathematical graph model, where the flip-flops are represented by nodes and the interconnecting wires by edges. The weights of edges are derived from the distances between flip-flops. It is evident that if a graph represents a scan chain it has to be a path.

Then the optimization problem can be transformed to traveling salesman problem which is very similar to our problem, except of the requirement to return back to the starting node. Traveling salesman problem is NP-hard problem [10]. To solve it, we can not use an exact algorithm because the best known exact algorithm has computational complexity in time of $O(2^n)$ (n is count of nodes) [11], [12] and scan chain may have thousands of flip-flops, the computational time would be unacceptable.

Therefore, it is necessary to use a heuristic or approximation algorithms such as Lin-Kernighan algorithm, simulated annealing or genetic algorithms. In the first stage we choose a simple greedy "nearest neighbour" algorithm which is very easy to be implemented and converges very quickly (less than 0.5 s). Even if the solution given by this algorithm was not excellent, it was sufficient to prove that the hypotheses are right. However we were expecting better results, so we tried to use a methodology which uses better solution of traveling salesman problem.

We chose an improved version of the Lin-Kernighan algorithm, the Concorde software package[2][13] which incorporates the limited neighborhood structure as well as an additional optimizations. Concorde is widely regarded as the fastest TSP solver for large instances. It uses the chained Lin-Kernighan algorithm and search depth is greatly limited but high quality is obtained by repeatedly applying double-bridge transformations and optimization. It also applies a simple algorithm to generate a fair quality initial tour that provides a large speed boost to the LK algorithm.

It was recognized that the Concorde algorithm eliminated problematical long wires and the total length of scan chains interconnections was reduced to 30 – 45 % of original total length.

This improved reordered scan chain was included into original circuit and new reroute process was performed, the results are described in the following section.

IV. Experimental Results

The method of optimization was verified on several real circuits which were gained from a company doing professional designs (see EXPER 01 – EXPER 04 in TABLE I - II). The original parameters are available in TABLE I. These are the results which represent the solution after the physical layout was developed by a professional design system and set of test vectors generated.

[2]freely available for academic research use

The results gained by our optimization procedure are shown in TABLE II.

The results prove that the hypotheses were correct and the method really allows to reduce the number of wires on which bridging faults can appear. In our experiments we took into account just the connections belonging to scan chain, the connections belonging to functional logic are excluded from the experiments. Then, after the reorganization was performed, the reduction of bridging faults was about 65 % of the value before the optimization. The reduction of bridging faults when all connections are considered (i. e. including the connections in functional logic) is about 96 – 98 % while the number of test vectors was reduced to 92 – 97 %. This difference is caused by unequal testability parameters of each component and its functional logic in terms of controllability/observability values.

The test application time reduction was evaluated for the situation when the shift of test vectors/responses to them through scan chain is synchronized with 20 MHz clock frequency.

V. Conclusions and Future Research

In this paper, the methodology which can reduce costs of postproduction testing by reducing the number of faults for which the circuit must be tested, is presented. This methodology is based on scan chain reordering to reduce length of connections between flip-flops. For the purposes of the research, a software tool was developed which allows to visualize results of physical scan chain flip-flop placing and their order in chain. To reorder scan chain we used the methodology known as traveling salesman problem and for solving this problem we used Concorde software package. The described method was tested on several real circuits and the test results confirmed that the approach really reduces the number of bridging faults which can appear in the structure. The reduction of test vectors amount and reduction of test time was confirmed as well.

The reduction of 3 – 8 % may seem as not very significant, but this relatively small improvement is useful in mass production because it reduces testing cost and time needed to apply the test.

We also found out from results that the methodology has probably better results for larger circuits with more scan chains, but we need more test circuits to prove it.

In our future research we shall concentrate on the analysis of circuit physical layout and checking whether real wire length after place and route process is approximately proportional to distance between flip-flops we used in algorithm (Manhattan metric). To improve the results we shall modify this metric so that it penalizes routes which are short but in route way there are many other wires which cause many other vias to appear between layers in the final layout which are predisposed to open-wire faults.

The objective of our research is to improve this methodology by taking other criterions of scan chain reordering into account and solve it as a multi-criterial problem. We

TABLE I
TEST CIRCUITS PARAMETERS BEFORE OPTIMIZATION.

Circuit	EXPER 01	EXPER 02	EXPER 03	EXPER 04
Number of gates	41 821	28 565	16 136	45 880
Number of scan chains	2	1	1	2
Number of flip-flops	2 285	1 129	745	2 173
Total number of bridging faults (functional logic + scan chain)	1 799 924	1 350 334	887 508	2 508 410
Number of bridging faults in scan chain connections	183 592	156 638	105 613	253 348
Total number of test vectors	820	459	1 134	2 175
Test time	46.92 ms	25.97 ms	42.28 ms	118.27 ms

TABLE II
RESULT OF OPTIMIZATIONS.

Circuit	EXPER 01	EXPER 02	EXPER 03	EXPER 04
Total number of bridging faults (functional logic + scan chain)	1 736 926	1 321 976	867 670	2 405 565
Number of bridging faults in scan chain connections	115 762	106 758	66 932	158 849
Total number of test vectors	764	439	1 102	2 005
Test time	43.72 ms	24.84 ms	41.09 ms	109.03 ms
Ratio of total number of bridging faults after/before optimization	96.5 %	97.9 %	97.8 %	95.9 %
Ratio of bridging faults in scan chain connections after/before optimization	63.1 %	68.2 %	63.4 %	62.7 %
Ratio of total number of test vectors after/before optimization	93.2 %	95.6 %	97.2 %	92.2 %
Total test time reduction	3.2 ms	1.13 ms	1.19 ms	9.24 ms

expect that through its optimization, it will result in additional reduction of testing time. One of these criterions can be a preference of placing flip-flops which are inputs to D/A convertor at the beginning of scan chain. Then, during testing D/A convertor it will not be necessary to shift test vector through the complete scan chain but it is enough to shift in the test vector representing the input to D/A converter. Similarly, it is useful to place flip-flops which are the outputs of A/D convertors or analog comparators to the end of scan chain. Then, just the bits representing the A/D output will be shifted out.

The goals of our research can be summarized in the following: we try to reduce scan chain test by decreasing the number of faults to which it is susceptible and by its reorganization. As a result, time needed to test circuit can become shorter which has importance in mass productions of electronic components where production costs can be possibly decreased significantly by this methodology.

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REFERENCES

[1] M. T. Schmitz, B. M. Al-Hashimi, and P. Eles, *System-Level Design Techniques for Energy-Efficient Embedded Systems*. Norwell, MA, USA: Kluwer Academic Publishers, 2004.

[2] M. Abadir and M. Breuer, "A knowledge-based system for designing testable vlsi chips," *IEEE Des. Test*, vol. 2, no. 4, pp. 56–68, 1985.

[3] S. Makar, "A layout-based approach for ordering scan chain flip-flops," in *International Test Conference 1998 Proceedings*, Washington, DC , USA, 1998, pp. 341–347.

[4] S. Chakravarty and V. Dabholkar, "Minimizing power dissipation in scan circuits during test application," in *IEEE International Workshop on Low Power Design*, 1994, pp. 51–56.

[5] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector ordering technique for switching activity reduction during test operation," in *GLS '99: Proceedings of the Ninth Great Lakes Symposium on VLSI*. Washington, DC, USA: IEEE Computer Society, 1999, p. 24.

[6] J. Skarvada, "Digital Systems Test Application Optimization for Low Power Consumption," Ph.D. dissertation, Brno University of Technology, 2009.

[7] W. Li, S. Wang, S. T. Chakradhar, and S. M. Reddy, "Distance restricted scan chain reordering to enhance delay fault coverage," in *VLSID '05: Proceedings of the 18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design*. Washington, DC, USA: IEEE Computer Society, 2005, pp. 471–478.

[8] R. A. Rutenbar and J. M. Cohn, "Layout tools for analog ics and mixed-signal socs: a survey," in *ISPD '00: Proceedings of the 2000 international symposium on Physical design*. New York, NY, USA: ACM, 2000, pp. 76–83.

[9] E. Larsson, *Introduction to Advanced System-on-Chip Test Design and Optimization*. Dordrecht, The Netherlands: Springer, 2005.

[10] D. L. Applegate, R. E. Bixby, V. Chvatal, and W. J. Cook, *The Traveling Salesman Problem: A Computational Study (Princeton Series in Applied Mathematics)*. Princeton, NJ, USA: Princeton University Press, 2007.

[11] S. Kohn, A. Gottlieb, and M. Kohn, "A generating function approach to the traveling salesman problem," in *ACM '77: Proceedings of the 1977 annual conference*. New York, NY, USA: ACM, 1977, pp. 294–300.

[12] R. M. Karp, "Dynamic programming meets the principle of inclusion and exclusion," *Operations Research Letters*, vol. 1, no. 2, pp. 49 – 51, 1982.

[13] D. Applegate, R. Bixby, V. Chvatal, and W. Cook, "Concorde – a code for solving traveling salesman problem." [Online]. Available: http://www.tsp.gatech.edu/concorde.html