Review of the Dissertation Thesis

Thesis title: Addressing Issues in Research on Packet Classification in Core Networks
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The Dissertation thesis deals with packet classification in core networks. Packet classification rules are first analyzed, both for IPv4 and IPv6 protocols. Then, a novel FPGA-based packet classification architecture able to cope with the 100Gbps throughput is designed. Actually, the achieved throughput is much higher. Finally, a new open source synthetic rule set generator was proposed, for benchmarking purposes.

Since the speed of networks is ever increasing, there is an urgent need of faster packet classification algorithms and hardware architectures implementing them. Moreover, their accuracy must be increased, mostly because of growing data volume. These issues are addressed and solved in the Thesis. Thus, the thesis topic is timely without doubt.

The contribution of the thesis is significant; it advances the state-of-the-art in many aspects, as mentioned below.

The summary of the Thesis is given below, with potential questions and comments embedded.

Section I presents the introduction and thesis goals. These can be summarized as:

- **Increasing the packet classification performance** (speed), in order to cope with the 100Gbps throughput for IPv4 and IPv6 protocols.
- **Benchmarking of packet classification** algorithms, in order to assess their efficiency.

Section II introduces the problem of packet classification in core networks. Definitions and use cases are stated, with a description of packet classification approaches. The section is finalized with required research issues, which correspond to the main topic of the Thesis.

When reading this section, I was missing references to works, where the listed approaches are implemented (used), but this is compensated in Section 3.

Q: In the algorithms benchmarking, only the classification speed and memory requirements are addressed as benchmarking goals. What about the classification accuracy?

Section 3 describes the related work. One-dimensional and multidimensional packet classification algorithms are reviewed, with their advantages and drawbacks. Next, available synthetic IPv6 rule set generators used for benchmarking classification algorithms are described.

Section 4 describes the first contribution of the Thesis – increasing the performance of packet classification in core networks. Particularly, the prefix matching implemented in FPGA is accelerated. A trie-based representation of a prefix set together with a pipelined hardware architecture for prefix matching based on this representation in an FPGA is proposed. The pipelined architecture is based on the "fetch-decode-execute" paradigm.

Q: Could you provide more details of the FPGA architecture shown in Figs. 4.3 and 4.4? I.e., the internal structure of the individual blocks? Even though their function is described in the text, the description seems to me to be too brief, in the implementation context.

Comment: I'm not sure about the claimed similar amount of resources and higher frequency of the implementation in newer FPGA chips. Just because of this involves using Xilinx Vivado instead of ISE. From my experience, Vivado has (surprisingly) worse logic synthesis than ISE, which may yield even worse results. Of course, the frequency should be increased by the newer technology used. However,

the area consumption can be higher. This heavily depends on details of the architecture, as commented in the question above. It would be nice to see the comparison. However, I definitely do not demand it.

Q: What was the ISE synthesis effort selected for the implementation? In the standard setting, ISE tries to make some compromise between the area and delay. If an increased area or delay optimization effort was chosen, the results will probably be different. Btw., what is your main target? Area or delay? I suppose it should be the delay, thus, the synthesis should be driven towards decreasing the delay. The area is insignificant, until the design fits into the FPGA. What is the motivation behind reducing the FPGA memory consumption? Again, when the design fits into the FPGA, the resources consumption needs not be of concern.

Nevertheless, the comments and questions raised above do not deny the obtained advantages of the proposed architecture, with respect to the state-of-the-art. I really do appreciate the obtained results.

Section 5 addresses the problem of benchmarking of packet classification algorithms. The ClassBench-ng tool generating synthetic IPv4, IPv6, and OpenFlow 1.0.0 rule sets is introduced. The efficiency and accuracy of the generator is proven by comparison with other tools.

Section 6 concludes the Thesis. The contributions are briefly summarized and proposals for the future work are made.

Publication activity

The results of the Thesis were published at eight international conferences, three workshops, and in one technical report. Even though no journal papers were produced, the applicant's publication activity can be assessed as very good.

Comments to the Dissertation Thesis text

The text is very well written and easy to read. There are minimum grammar mistakes, mostly just typos.

Judging from the above, it can be concluded that the applicant is highly scientifically qualified. He has proven the ability to conduct his own research and publish the results at very good conferences. Therefore,

I do recommend

the submitted thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

In Prague, 22. 3. 2019

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