Review of the Dissertation Thesis

Thesis Title: Automated Design Methodology for Approximate Low Power Circuits
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The Dissertation thesis proposes CGP-based methods for low-power approximate circuits design. Particularly, the main objective of the research was to show that by using CGP based circuit approximation algorithms, it is possible to reduce the power consumption of digital combinational circuits described at various levels of abstraction.

The Thesis is constructed as a collection of seven selected papers with common introduction and summary sections.

The thesis topic just follows one of the most recent research areas: the design of approximate circuits, mostly targeted to decrease power consumption. In this sense, the thesis topic is timely without doubt.

The contribution of the thesis is really significant, it advances the state-of-the-art in many aspects, as mentioned below.

The main contributions can be summarized as:

1. **New methods to design approximate circuits at different levels of abstraction**, from the transistor-level design up to RTL level. All these methods are based on Cartesian Genetic Programming (CGP).
2. **New simulation methods** of CGP candidate solutions.
3. **New formal methods to evaluate the CGP candidate fitness and power consumption.** These methods are based on SAT and BDDs.
4. **Evaluation on practical designs.** Particularly, approximate arithmetic circuits (adders, multipliers), which are then incorporated in more complex designs, like neural networks, HEVC encoder, and image and signal filters.

In paper I., the CGP-based design of "small" digital (in contrast to well-studied analog) circuits constructed from transistors is proposed. A combined simulation model (analog and discrete multi-valued event-driven simulation) is used to evaluate the quality of the candidate solutions. As a result, novel transistor-level (non-CMOS) structures were evolved. This idea was further extended in another paper [38] by estimation of the power consumption, so it can be minimized. Design of approximate circuits at transistor-level was proposed in [38] too. I'm missing this paper in the Thesis text.

Paper II. presents a CGP-based design of approximate arithmetic circuits, constructed at gate-level. The obtained library of generated solutions has been made available for general publics, for design and benchmarking purposes.

Low-power approximate multipliers were applied to neural networks design in Paper III. The "accurate zero-multiplication" constraint was applied, as a remedy to poor performance of the original approximate implementation. As a result, a significant power reduction was achieved, with just slight classification accuracy degradation.

SAT-based CGP fitness computation with a special miter was presented in Paper IV. By this method, approximate arithmetic circuits with guaranteed error and good error/size tradeoffs were produced.

In Paper V., the author proposes a low-power HEVC encoder. Reduced power consumption is achieved by application of approximate adders and subtractors. BDDs are used to derive the approximation error and switching activity.

Journal paper VI. studies the influence of base gates/cells used in CGP in the context of approximate logic design, particularly design of approximate adders and multipliers.

Finally, the journal paper VII. studies approximation at higher level of abstraction, up to the software level. Approximate lower power consumption and execution time is sought. Low-power median networks were evolved by CGP. The evolved architectures were then evaluated on median filters implemented in a microcontroller.

Apart from the seven above-mentioned papers (5 at prestigious conferences, 2 journal papers), the applicant has been a co-author of 12 conference papers, one journal paper and three student workshop papers. Thus, his publication activity is outstanding.

The applicant participated in seven research projects (from which three were GACR projects).

Comments to the Dissertation Thesis text

The text is well written and easy to read. The introduction and state-of-the-art sections allow-non expert readers to understand the content and context.

There are minimum grammar mistakes, mostly just typos.

Even though all the papers are relatively well commented, I would appreciate more detailed summaries of their content and outcomes, i.e., more thorough descriptions of the main principles and presentations of concrete results. Even though it is seen what has been done in individual papers, details are omitted. As a result, one has to read all the papers in order to understand the principles and see detailed results.

Minor comments:

- In Subsection 2.1.3 you speak about clock gating in combinational circuits. Even though the principle is clarified, it should not be called "clock gating". There are no references to papers dealing with this issue.
- Subsection 2.1.3: there are many other logic synthesis techniques reducing the power consumption, which are not mentioned there. See, e.g.,
    - A. P. Chandrakasan and R. W. Brodersen, "Minimizing Power Consumption in Digital CMOS Circuits", Proceedings of the IEEE, Vol 83, No. 4, April 1995.
    - S. Das, P. Dasgupta, P. Fišer, S. Ghosh, D. K. Das, "A Rule-Based Approach for Minimizing Power Dissipation of Digital Circuits," in Proc. of 19th DDECS, 2016, pp. 237-242.

Questions to the discussion

1. Why haven't you included paper [38] in the Thesis text? I think it is quite important.
2. The approximate multipliers used in the neural networks may introduce non-linearity. Isn't it a problem for the learning algorithm?
3. Paper V.: have you considered using a SAT-based approach for computing the error (like in paper IV.) instead of BDDs? I think it could do the same job, maybe in a more efficient way. Even #SAT could be applicable.

Judging from the above, it can be concluded that the applicant is highly scientifically qualified. He has proven the ability to conduct his own research and publish the results at very good conferences and impacted journals. Therefore,

I do recommend

the submitted thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

In Prague, 10. 9. 2018

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