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NOVEL APPROACH TO POLYMORPHISM IN GATE-LEVEL DIGITAL CIRCUITS
NOVÝ PŘÍSTUP K POLYMORFISMU ČÍSLICOVÝCH OBVODŮ NA ÚROVNI HRADEL

PHD THESIS
DISERTAČNÍ PRÁCE

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Abstract

Nearly twenty years ago, a non-conventional approach to implementation of multifunctional circuits called polymorphic electronics was proposed. The concept of polymorphic electronics allows to implement two or more functions in a single circuit, whereas the currently selected function depends on the state of the circuit operating environment. Key components of such circuits are polymorphic gates. Since the introduction of polymorphic electronics, several dozens of polymorphic gates have been published. However, a large number of them do not meet reasonable parameters. As a result, perspective of their utilisation for real applications becomes rather bleak. This dissertation introduces a new approach to the polymorphic electronics. It is based on gates whose behaviour depends on polarity of dedicated power supply rails. The goal of this thesis is to show that such approach allows to design gates with significantly better parameters. In order to systematically design proposed gates at the transistor level, an evolutionary method based on Cartesian genetic programming was proposed. That allowed to design several sets of efficient polymorphic gates employing conventional MOSFET and emerging double-gate ambipolar transistors. These gate sets were arranged into a library which is currently freely available for other researchers. Furthermore, a number of more complex circuits based on proposed gates were designed in this thesis. It is demonstrated at various levels of circuit design (gate, RTL, application) that the proposed gate-level polymorphism provides significant advantages compared to the first generation of polymorphic gates, but it can also be competitive or even better compared to the conventional CMOS solutions.

Keywords

Polymorphic electronics, multifunctional gate, polymorphic gate, ambipolar transistor, MOSFET, digital circuit, PoLibSi.

Reference

Abstrakt

Před necelými dvaceti lety byl představen nekonvenční přístup k implementaci multifunkčních obvodů, tzv. polymorfní elektronika. Polymorfní elektronika umožňuje implementovat jedním obvodem dvě nebo více funkcí, přičemž aktuálně funkce závisí na stavu okolního prostředí obvodu. Klíčovými komponentami takových obvodů jsou polymorfní hradla. Od představení konceptu polymorfní elektroniky bylo publikováno několik desítek polymorfních hradel. Parametry většiny z nich však neumožňují jejich využití v reálných aplikacích. Bez dostatečného množství polymorfních hradel s dobrými parametry však nejspíše zůstane v aplikacích založených na multifunkčním chování nebo rekonfiguraci konvenční elektronika preferována před tou polymorfní. Tato disertační práce představuje nový přístup k polymorfní elektronice. Je založen na hradlech, jejichž funkce závisí na polaritě napájecích přívodů. Cílem této disertační práce je ukázat, že takový přístup umožňuje navrhnout hradla s výrazně lepšími parametry. Aby bylo možné systematicky navrhovat na úrovni tranzistorů takováto hradla, byla navržena evoluční metoda založená na kartézském genetickém programování (CGP). To umožnilo navrhnout několik sad efektivních polymorfních hradel založených jak na konvenčních MOSFET tranzistorech, tak na double-gate ambipolárních tranzistorech. Z těchto sad hradel byla vytvořena knihovna, která je v současné době volně dostupná pro ostatní vědce. Dále byla v této práci navržena řada složitějších obvodů založená na navržených hradlech. Na různých úrovních návrhu obvodů (hradla, RTL, cílová aplikace) je pak ukázáno, že navrhovaný polymorfismus na úrovni hradel představuje velké výhody v porovnání s předchozí generací polymorfních hradel, ale může být také konkurenceschopný nebo výrazně lepší než konvenční řešení takovýchto obvodů.

Klíčová slova

Polymorfní elektronika, multifunkční hradlo, polymorfní hradlo, ambipolární transistor, MOSFET, číslicový obvod, PoLibSi.

Citace

Rozšířený abstrakt

Před necelými dvaceti lety byl představen koncept tzv. polymorfní elektroniky. Polymorfní elektronika umožňuje nekonvenčním způsobem implementovat multifunkční číslicové obvody. Především ty, u nichž se předpokládá jedna hlavní a jedna či více pomocných funkcí, které se aktivují jen za určitých podmínek okolního prostředí obvodu (teplota čipu, napájecí napětí apod.). Cena takto přidané funkce k obvodu může být v případě polymorfní elektroniky nízká. Polymorfní elektronika tak může najít uplatnění např. oblasti diagnostiky, bezpečnosti a mnoha dalších.

Klíčovými komponentami takových obvodů jsou polymorfní hradla. Od představení konceptu polymorfní elektroniky bylo publikováno několik desítek polymorfních hradel, často řízených velikostí napájecího napětí, teplotou čipu nebo speciálním signálem. Parametry většiny z těchto hradel jsou však výrazně horší než parametry konvenčních CMOS hradel a parametry CMOS obvodů, které realizují obdobnou funkci jako ty polymorfní, ať už jde o jejich velikost, zpoždění nebo spotřebu. To znemožňuje využití polymorfní elektroniky v reálných aplikacích. Bez dostatečného množství polymorfních hradel s dobrými parametry by tak konvenční řešení nejspíše zůstala upřednostňovaná před polymorfní elektronikou ve všech aplikacích založených na multifunkčním chování nebo rekonfiguraci.

Tato disertační práce představuje nový přístup k polymorfní elektronice. Je založen na hradlech, jejichž funkce závisí na polaritě napájecích přívodů. Cílem této práce je ukázat, že takovýto přístup umožňuje navrhnout hradla s výrazně lepšími parametry a že polymorfní obvody sestavené z těchto hradel mohou být konkurenceschopné konvenčnímu řešení obvodů se stejnými funkcemi.

Aby bylo možné takováto hradla na úrovni tranzistorů systematicky navrhovat, byla navržena evoluční metoda založená na kartézském genetickém programování a diskrétní simulaci kandidátních řešení. Ač je v této práci použita pro návrh obvodů postavených na MOSFET nebo double-gate ambipolárních tranzistorech, při vytvoření vhodných tranzistorových modelů není konkrétním typem tranzistorů limitována.

Pomocí navržené metody bylo vytvořeno osm úplných sad dvouvstupých polymorfních hradel řízených polaritou napájecího napájení s ohledem na různá kritéria (velikost, zpoždění, spotřeba). Jelikož bylo ukázáno, že takovéto obvody nejsou funkčně úplné, pokud není v obvodu dostupná nějaká konstantní logická úroveň, bylo předpokládáno, že v polymorfních obvodech konstantní logické úrovně dostupné jsou, např. v podobě dalších dvou napájecích přívodů o neměnném potenciálu.

Z navržených sad hradel byla vytvořena knihovna PoLibSi, která je volně dostupná online. Každá sada publikovaných hradel je úplná – obsahuje alespoň jednu efektivní implementaci libovolné kombinace dvouvstupých Booleovských funkcí, což může přispět k efektivnější syntéze složitějších obvodů. Každé hradlo je v knihovně reprezentováno pomocí HSPICE zápisu, obsahuje schéma, výsledky simulací a v případě hradel založených na MOSFET tranzistorech i jejich spotřebu a zpoždění.

Bylo ukázáno, že všechna hradla navržená s ohledem na co nejmenší rozměry jsou co do počtu tranzistorů menší než realizace takovýchto obvodů pomocí dvou (mono-funkčních) obvodů a jednoho multiplexoru a že jsou často stejně velká či dokonce ještě menší než implementace obou funkcí hradla odděleně (tj. bez multiplexoru).

Parametry hradel založených na double-gate ambipolárních tranzistorech nebyly (kromě velikosti) dále zkoumány, neboť nebyly v době výzkumu volně k dispozici jejich SPICE-kompatibilní simulační modely. Parametry hradel založených na MOSFET tranzistorech se ukázaly výrazně lepší oproti parametrům předchozí generace polymorfních hradel. Hradla ze setu optimalizovaného současně na nízkou spotřebu a malé zpoždění se pak ukázala

konkurenceschopná i konvenčním řešením takovýchto obvodů ve všech zkoumaných ohledech (velikost, zpoždění i spotřeba). Problém polymorfní elektroniky s nedostatkem hradel s dobrými parametry je tak dobře řešitelný – knihovna PoLibSi obsahuje hradel dokonce 38117.

Tato práce dále demonstruje, že úplné sady efektivně implementovaných hradel mohou přispět k redukci velikosti složitějších obvodů. Bylo implementováno několik aplikací a několik desítek RTL komponent založených na navržených hradlech. Polymorfní RTL komponenty byly o 14.3 – 49.1 % menší v porovnání se state-of-the-art implementacemi založenými na předchozí generaci polymorfních hradel. Dvoufunkční grafické filtry pak o 30 – 39 % menší než implementace založené na předchozí generaci polymorfních hradel a o 19 – 34 % menší než implementace založené na konvenčních (mono-funkčních) hradlech.

Výsledky v této práci tak ukazují, že polymorfní elektronika může být opravdu koncept, který je schopný vylepšit efektivitu implementace obvodů s jednou sekundární funkcí co se týká výsledné velikosti obvodu, a to nejen v akademické sféře, ale i v praxi.

Novel approach to polymorphism in gate-level digital circuits

Declaration

Hereby I declare that this PhD thesis was prepared as an original author's work under the supervision of doc. Ing. Richard Růžička, Ph.D., MBA. The supplementary information was provided by Ing. Vojtěch Mrázek, Ph.D. and doc. Ing. Zdeněk Vašíček, Ph.D. All the relevant information sources, which were used during preparation of this thesis, are properly cited and included in the list of references.

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Jan Nevoral
September 9, 2019

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Contents

Chapter 1

Introduction

Nowadays, significant majority of logic circuits is typically realised by means of using widespread CMOS technology. Although the first physical implementation of CMOS-based logic circuit has been successfully demonstrated more than 55 years ago [71], this technology still prevails as the major choice even in case of cutting-edge electronic devices.

In fact, last several decades have brought only a minor advancement regarding the structural and implementation aspects of basic Boolean functions (logic gates) in CMOS technology. When it comes to the target implementation size of logic circuitry, CMOS gates seem to be very optimal (only a few transistors are needed to implement a Boolean function). Thus, even very complex behaviour can be realised on a small silicon die.

In certain classes of applications, it is required to have more different functions implemented in a single circuit, whereas just one of them is always active. In such situations it makes sense to think about optimisation of the circuit size. The easiest possible implementation of such a circuit is to implement all functions separately on the silicon die and to switch their outputs according to the current needs. In order to accomplish higher functional density (more features within a similar chip area or number of transistors), the reconfiguration scheme is sometimes utilised [7].

Reconfigurability brings more effective ways how to implement certain applications and allows new applications of electronics. It makes the hardware more flexible. This is one of the features that make software so popular as a way to implement various systems. However, a wide range of applications still needs to be implemented in hardware. Thus, the reconfiguration is (and will be henceforward) very important for a significant class of applications.

Typical implementation of hardware reconfiguration consists of a field of reconfigurable elements connected by a changeable interconnection network, a reconfiguration controller and a memory that serves as a storage for different configurations. This approach allows to implement two or more digital circuits using one hardware. The field of reconfigurable elements might usually assume various granularity levels – from coarse-grained elements like functional units or data processing units on RT level to a transistor-level fine-grained field of elements [78]. It allows not only the classic reconfiguration scheme (the hardware changes its structure and behaviour according to the configurations created beforehand), but also implementation of so-called evolvable hardware (new configurations are being created just as a direct response to the actual circumstances) [28].

The flexibility of described reconfiguration approach is paid by overhead in the time domain. The change of function consumes certain period of time. It is caused by presence of only one hardware (field of configurable elements) for more configurations. Previous

configuration must be replaced by a new one. Naturally, some space is also required for the reconfigurable circuit, the memory and the reconfiguration controller.

In 2001, Stoica et al. proposed somewhat non-conventional approach to the implementation of multifunctional digital circuits called *polymorphic electronics* [64]. This approach could be understood as another (and quite different) conception of hardware reconfiguration. On the contrary to the conception of classic reconfiguration, where reconfigurable elements are connected by means of an universal interconnection network, polymorphic circuits look like ordinary digital circuits (just tightly coupled elements) and the change of the circuit function is triggered only by the change of behaviour of its elements (typically gates). If these multifunctional elements are implemented effectively and the circuit synthesis is performed cleverly, the final circuit is very efficient in both area and time domains. In fact, the function change is almost immediate and, moreover, overhead in the size domain for an additional circuit function could also be very low. Neither additional memory nor any reconfigurable controller or reconfigurable network is needed.

1.1 Polymorphic electronics

Polymorphic electronics [64] can be characterised as a relatively new discipline in the field of digital circuits and systems. Its notion depicts a group of digital circuits that have the ability to perform more than one function, while the wiring of a given circuit keeps the same layout in all the intended operating modes. Selection of the corresponding function, which the circuit is going to execute, depends on the actual state of the target operating environment. Because the basic building blocks of polymorphic electronics (polymorphic gates) are sensitive to the target operating environment directly, there is no need for any central reconfiguration controller, nor any dedicated control signal connected to all multifunctional components, which would cause the reconfiguration. That increases the efficiency in implementation of polymorphic circuits.

All modes (functions) of the polymorphic circuits are designed inside the circuits completely intentionally. No mode results from any fault, caused e.g. by exceeding operating parameters of the circuit. Polymorphic circuits are usually synthesised from the polymorphic gates. The change of function of the whole circuit is caused by the change of Boolean functions performed by individual polymorphic gates. In the first generation of polymorphic gates, the change of gate function was reached by the change of operating points of the employed transistors – by such factors or environment, which influence the operating points of transistors. It can be physical quantities like a supply voltage level [45, 61, 65, 63], voltage of a dedicated control signal [42, 64, 75, 76], chip temperature [48, 62, 64, 70] or even its illumination [64].

Interconnection of all circuit components remains always the same. Switching of the circuit modes (functions) happens thus naturally and immediately. There is no need to wait for completion of any reconfiguration or any other sequential operation. Because the detection of environment state is a built-in feature of the individual gates themselves, no part of the polymorphic circuits can be identified as a sensor, which is sensitive to the physical quantity and which would serve for distribution of the measured values into the remaining parts of the circuit. Polymorphic circuits could be thus much smaller than similar circuits created by conventional design methods (circuits consisting of several monofunctional blocks and multiplexers) in terms of the overall number of transistors or layout size [44].

Although the concept of polymorphic electronics generally admits several equally important functions implemented in a single circuit, just one main and one or more auxiliary functions are often considered in practice. The mechanism responsible for the change of polymorphic circuit function implies the existence of some application domains, in which such kind of behaviour may help to get significant advantages. In general, these circuits can be used e.g. for adaptation of the circuit behaviour to variable conditions of target environment [43], for reduction of power consumption or heat dissipation in order to preserve at least the essential circuit functionality, when energy goes low or temperature goes high [46], for storing or hiding „extra" functions used as a watermark or other special features [53], for embedded diagnostics [55], etc. Note that the environment could be both intentionally driven (to initiate the reconfiguration) or utilised as a driver of change (the circuit responds to changed circumstances).

1.2   Open problems of polymorphic electronics

The characteristic features of polymorphic electronics described above show the advantages, which could be useful for instance in certain classes of circuits, which require to change their function during the runtime. Thus, polymorphic electronics seems like a perspective research area.

Since 2001, several tens of publications have been devoted to the field of polymorphic electronics. There were designed more than thirty building blocks for polymorphic circuits (usually polymorphic gates). Two of them were even fabricated and tested with real applications of polymorphic electronics. Furthermore, several methods for synthesis of polymorphic circuits were created. A detailed state-of-the-art in polymorphic electronics is given in Chapter 2 of this thesis.

In general, a research related to the polymorphic electronics focuses on three problems of polymorphic electronics [44]:

1. Existence of suitable polymorphic components (usually polymorphic gates) with parameters competitive to the parameters of conventional gates used in the digital circuits.

2. Design of more complex polymorphic circuits using the basic components (i.e. problem of synthesis methods, which should be reliable, scalable, etc.).

3. Identification of appropriate classes of applications, where the polymorphic electronics could be more beneficial than a conventional solution.

1.3   Research objectives

This thesis deals with the first mentioned problem of polymorphic electronics – with design of the polymorphic gates as basic building blocks for polymorphic circuits.

One of the main issues behind the adoption of polymorphic electronics is given by the analogue nature of the phenomenon (quantity) influencing the circuit behaviour. It consequently leads to rather analogue design concepts of the polymorphic gates rather than staying in a purely digital domain (see Chapter 2.3). The result is that some transistors work in a linear mode or could short the power rails. That brings a lot of shortcomings (not all the published gates have all of the listed ones): High power consumption, high

propagation delay, output levels weak or even incompatible with CMOS voltage levels, long transient phenomenon, large size (in case of big differences in transistor sizes), etc. However, without enough polymorphic gates offering good properties, conventional electronics will be most likely the preferred way to polymorphic electronics in application scenarios targeting multifunctional behaviour or reconfiguration.

With the emergence of ambipolar transistors, a few bi-functional circuits were published, whose behaviour depends on the polarity of power supply voltage [73, 68]. Although such a principle seems to be promising due to the discrete nature of the control variable, it was not further investigated for design of the multifunctional digital circuits.

The following hypothesis was formulated for this thesis:

It is possible to design a complete set of two-input gates created from the existing types of transistors (MOSFET, ambipolar, etc.), where each gate in the set is able to realise two Boolean functions, where the current function is given by the polarity of the power supply rails, and where each gate from the set is better than a conventional solution of such bi-functional circuit (two conventional gates implemented in parallel + multiplexer) in terms of the overall number of transistors.

The main objective of the thesis can be divided to the following partial goals:

1. To identify possible issues or limitations related to the design of circuits controlled by the polarity of power supply voltage, if any.

2. To propose and implement a method which allows to design polymorphic circuits controlled by the polarity of power supply voltage at the transistor level, with regards to the overall transistor count.

3. To experimentally evaluate the proposed method using selected types of transistors and to tune and accelerate the design algorithm in order to speed up the circuit design process.

4. To design complete sets of two-input polymorphic gates for various types of transistors and various design constraints.

5. To evaluate other important non-functional properties of the proposed gates besides the number of transistors being used (e.g. propagation delay, power consumption).

6. To compare obtained results with the conventional implementations of such bi-functional circuits.

7. To show the advantages of proposed gate set(s) on selected applications of polymorphic electronics.

1.4 Motivation

There are two main motivations for the research connected with this thesis.

The first one is to create a set of gates with more efficient implementations (a new generation of polymorphic gates). Gates sensitive to some continuous quantity were designed by an analogue approach. That usually resulted in non-optimal parameters of such gates when attempting to keep the gates size small. Moreover, time for switching of the

circuit function could be (especially in large circuits controlled by the chip temperature) not negligible.

If the circuit function will be controlled by polarity of the power supply voltage, the behaviour of such circuit will be predictable most of the runtime due to a negligible time required for switching the polarity. Discrete nature of the control quantity could also simplify a design of such gates and could have a positive influence on their properties – all transistors can work as switches, transistors can have common dimensions, etc. That would lead to higher possible operating frequency, lower power consumption and operation without a transient phenomenon during the function change.

The second motivation is related to the synthesis of polymorphic circuits. Synthesis methods can be various in the future and therefore it is difficult to estimate which polymorphic nodes (gates) will be required by the methods. If the proposed set of gates will be complete (i.e. if the set will implement all possible combination of two-input Boolean functions), proposed gate set can be utilised by any synthesis method, regardless of the circuit representation (PolyBDD [19], PAIG [12], etc.). For each method, a suitable subset of gates can be selected.

1.5   Thesis outline

This thesis is composed as a collection of selected author's papers with an accompanying introductory part. Five accepted peer-reviewed conference papers encapsulate the contribution of this dissertation. All papers are attached in their original publication format.

The thesis is organised as follows. The first chapter introduces the research area and research objectives. Chapter 2 surveys the state-of-the-art in polymorphic electronics already published in the literature. Chapter 3 summarises the research contribution and introduces the selected papers. Finally, Chapter 4 summarises the obtained results.

Chapter 2

Survey of the state of the art

As it was already outlined in Chapter 1.2, three research areas can be identified in the field of polymorphic electronics: Identification of applications, where the polymorphic electronics can bring an advantage in comparison to the conventionally designed circuits, development of suitable synthesis methods and, finally, design of suitable polymorphic components (usually polymorphic gates).

This chapter summarises the current state-of-the-art in all three research areas. With respect to the objectives of this PhD thesis, the biggest attention is paid to the currently published polymorphic gates. Note that a detailed survey of the state-of-the-art in polymorphic electronics by 2011 can be found in Růžička's habilitation thesis [44]. Although, many papers related to the polymorphic electronics have been published later, no other publication summarising the state-of-the-art in the polymorphic electronics has been created since 2011.

2.1 Applications of polymorphic electronics

Polymorphic electronics is not inherently suitable for all kinds of applications, but we believe that it can bring some improvement or advantage over conventional solutions in certain classes of applications. One of the open problems of polymorphic electronics is the identification of such suitable classes of applications.

Several possible areas of application of polymorphic electronics are already mentioned by the Stoica's team in the publication which introduced polymorphic electronics [64]. The advantage is seen in circuits having one primary function, where it would be nice to have one or more other auxiliary functions, which can be used when needed. Polymorphic electronics could be the way how to add the secondary function(s) for a low additional price. The use of added functions could be primarily in security applications according to Stoica's team: Authentication mechanism or watermark for identification, protection against the reverse engineering, where the main circuit function only occurs under certain conditions, or protection against unauthorised use by encoding sensitive data into the circuit. The publication also mentions a potential in applications where faults tolerance needs to be increased or the circuit needs to be adapted to worse conditions such as decreasing supply voltage. However, no specific application was investigated by Stoica and his team. A high number of real applications were later shown by the team of scientists from Brno University of Technology.

Stareček et al. proposed a method for improving the testability of digital circuits, where the substitution of selected conventional gates by polymorphic gates allows to generate a significantly shorter test sequence (lower number of test vectors) to test the failures than it would be necessary when using the original gates [60]. Other applications in the field of test and diagnostics are the self-checking circuits [45], for example self-checking adders that provide error information within the circuit on their outputs in the second polymorphic mode [50].

Compact dimensions and the fact, that circuit function depends on the environment conditions, predetermine the use of polymorphic electronics also in applications where the system's collapse due to unfavourable environmental conditions (high chip temperature, low supply voltage, etc.) can be prevented by timely adaptation of its behaviour, e.g. reduction of power consumption. The team of A. Stoica came up with the idea of an application that will reduce the resolution and frequency of an A/D converter during adverse conditions [64], but it has never been realised.

Similar application was proposed and implemented e.g. by L. Sekanina et al. They published a FIR filter with two operating modes [51]. The first mode was considered as a standard mode in which the filter performs a normal operation. In the other one, the filter operates with reduced power supply voltage – some filter coefficients were reconfigured, and some parts of the filter were disconnected. The experimental results indicated that while power consumption can significantly be reduced when half of the taps is suspended, the filter is still able to achieve a reasonable quality of filtering.

Růžička presented a design approach to gracefully degrading digital circuits that provides an increased chip operation reliability when battery goes low or a chip temperature cross some safe level [43, 46]. It is based on a circuit controller which decreases number of its states in the second mode. After the end of reconfiguration phase, the controller ensures only necessary functions. By this arrangement, the power and heat dissipation of the circuit is reduced until the chip temperature falls again under certain level. When the chip is cooled down appropriately, the controller returns to normal operating mode automatically. The principles of polymorphic electronics ensured fast reconfiguration, compact and cost-effective design with embedded sensors.

Since the polymorphic electronics implements multiple functions within a single circuit and it is not possible to identify parts performing individual functions, polymorphic electronics can also be used in the field of circuit security. The device may have one more hidden function that can serve for instance to identify a particular instance of a circuit. This was demonstrated by implementation of the physically unclonable function producing a unique chip ID [53].

Other published applications are e.g. transition function of cellular automaton [58] or bi-functional graphic filters [54]. Implementations of the mentioned graphical filters were further significantly improved with use of gates controlled by the polarity of supply voltage by the author of this thesis (see Chapter 3.4).

Some polymorphic gates can also be successfully used as monofunctional gates in conventional circuit design. Gajda designed a 2-bit full adder and a five-input majority function where gates controlled by a dedicated signal were utilised as conventional three-input gates. Both solutions are more efficient than the conventional solutions in terms of the overall number of transistors being used [18].

Polymorphic electronics can also be used in sequential digital circuits. Sequential controllers intended for gracefully degrading digital circuits designed by Růžička [43, 46] mentioned above were designed using a combination of polymorphic combinational circuits and

conventional flip-flops. Stoica's team created polymorphic JK flip-flops assembled from a combination of conventional and polymorphic gates [77]. An asynchronous counter allowing up- and down- counting or counter reset (i.e. three different functions) according to the target environment is provided as an example of such flip-flop usage. Following the up- and down- counter, the author of this thesis proposed combinational increment/decrement (notation with slash is typical for polymorphic circuits; increment is a function in the first mode, decrement in the other one) and adder/subtractor circuits which can be used in a wide scale of polymorphic applications (see attached Paper V or [33]).

2.2 Synthesis of polymorphic circuits

The problem of polymorphic circuit synthesis lies in the efficient design of circuit having desired functions from the basic polymorphic components. This problem is more complex compared to the design of conventional circuits, since more than one circuit function needs to be considered, and one common graph (circuit structure) needs to be found for all functions. Only a change in the component behaviour ensures that the circuit function is changed. This significantly reduces number of solutions in the (large) state space.

Small and simple polymorphic circuits can be designed by the *ad-hoc* approach directly by hand, just using the designer experience. However, most of the gates and circuits presented in Chapters 2.1 and 2.3 are results of the evolutionary design. Evolutionary techniques are sometimes able to find unconventional, interesting, yet functional solutions – both in the design and optimisation of digital systems [49]. It is done by searching in the state space using techniques based on Darwin's idea of gradual evolution of species with natural selection. Cartesian Genetic Programming (CGP) [29] was utilised for representation of almost all complex polymorphic circuits during the design. A high number of publications are focused on evolutionary design and optimisation of polymorphic circuits at both the transistor [65, 74, 34, 36, 35] and gate level [19, 54, 56, 79, 23]. Unfortunately, evolutionary methods are poorly scalable. Finding of more complex circuits requires larger chromosomes and thus searching in a larger state space. That makes finding of a suitable solution very time-consuming task and the probability of the finding decreases.

Synthesis methods that do not use any evolutionary algorithm nor any other heuristics to search the state space can be called as conventional. Two conventional synthesis methods were proposed by Gajda in his PhD thesis [17]. The simplest one is *polymorphic multiplexing*. It is based on polymorphic multiplexers (pmux) which propagate first input signal in the first mode and the other signal in the second mode, according to the current state of the target environment. A conventional approach is used to synthesise both circuit functions independently. The outputs of the synthesised circuits are then multiplexed using polymorphic multiplexers as shown in the left part of Figure 2.1. In order to reduce the number of gates, goal of the synthesis can be to maximise the amount of gates that are shared by both circuits (see the intersection in the right part of Figure 2.1). The other method proposed by Gajda, *PolyBDD*, is based on binary decision trees. Both methods generate functional circuits. However, it may not be optimal in terms of circuit size, so Gajda recommends the subsequent use of evolutionary optimisation techniques to obtain more optimal circuits.

Another three conventional synthesis methods were proposed by Adam Crha. The first one is based on formal Boolean representation of corresponding functions and can be successfully used for technology mapping of small polymorphic circuits for platforms based on NAND/NOR gates [10], e.g. for REPOMO32 [52]. The second method is based on
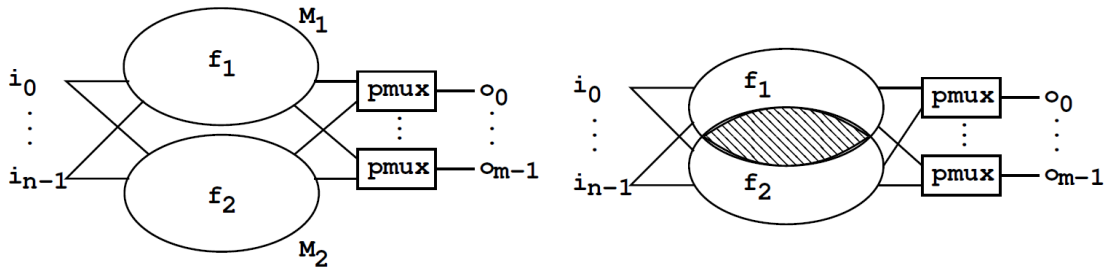
Figure 2.1: Multiplexing of conventional circuits by polymorphic multiplexers: Independent circuits (left) and sharing gates between modules (right) [17].

Boolean divisor identification and function kernelling technique [11]. Unfortunately, the method allows also only two-level circuit representation (sum of products or products of sum) and it would be poorly scalable for complex polymorphic circuits.

It seems that the most promising synthesis method could be the last method proposed by Crha [13], where the circuit is represented by so-called PAIG format – AIG representation (And-inverter graph) extended by polymorphic edges. Optimisation of such circuit is done by rewriting – replacing 4-input 1-output parts of the circuit by more efficient implementations. For an efficient mapping from PAIG to the target technology, polymorphic gates with various functions can be useful, not just common AND/OR or NAND/NOR gates. The PoLibSi library (see attached Paper IV or [38]) created by the author of this thesis is suitable for this purpose because it provides an efficient implementation of each pair of two-input Boolean functions for three target technologies including the conventional MOSFET transistors.

2.3   Polymorphic gates

Digital circuits are mostly designed by a composition of smaller circuit structures. Parameters of such structures (delay, size, power consumption, etc.) are known during the synthesis. That can allow to generate circuits optimal for a given application. Such structures can be gates, flip-flops, various types of adders, multipliers, RTL components or for example memory cells.

Design of the polymorphic circuits is based on the same approach. As the basic components for design of polymorphic circuits, two-input gates are mostly considered. An example of larger circuit blocks can be found in [54] where 8-bit components (min/max, min/mean, max/add, etc.) were synthesised out of two-input gates.

For design of more complex polymorphic circuits, a combination of conventional and polymorphic two-input gates is mostly considered. In order to assess whether the polymorphic gates can be integrated into the conventional CMOS circuits, properties and criteria which should be fulfilled by polymorphic gates were defined in [44]. They correspond to the properties usually required from the conventional gates:

- high input resistance (the gate must avoid an excessive load applied to the preceding logic net caused by its inputs),

- low output resistance (the aim is to achieve unambiguously defined logic levels at the gate output irrespective of a given output load caused by subsequent logic net),

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- power supply voltage in the range typical for CMOS circuits,

- acceptance of input signal levels in the range typical for CMOS circuits,

- output signal levels in the range typical for CMOS circuits,

- short time of signal propagation,

- low power consumption,

- small dimensions.

All polymorphic gates published so far are briefly introduced in this chapter together with their properties (if known). Note that some of the presented gates were not marked by the term *polymorphic* originally by their authors. However, their behaviour is polymorphic and thus they are also included in the state-of-the-art.

The most natural classification of polymorphic gates is a classification according to the phenomenon the gates are controlled by, i.e. according to the quantity which primarily influences the gate behaviour. The first three sub-chapters are devoted to the gates belonging to the first generation of polymorphic gates: Gates controlled by supply voltage level, chip temperature or dedicated control signal, i.e. by continuous control variables. These phenomena were proposed already by Stoica et al. in the publication introducing polymorphic electronics [64]. Such gates are based on MOSFET transistors and mostly designed as analogue circuits. Only two of them have been fabricated so far. The rest was simulated or tested in a field programmable transistor array [78].

The emergence of so-called post-silicon devices (especially ambipolar transistors) opened a path towards gates controlled by the polarity of supply voltage. The following sub-chapter pays an attention just to these gates. Because of discrete nature of the control variable and because of significantly better properties of such gates, they can be classified as a second generation of polymorphic gates.

The last sub-chapter shows other gates based on unconventional structures, which could be denoted as polymorphic (or at least multifunctional).

2.3.1 Gates controlled by supply voltage level

One of the possible approaches, how to control the polymorphic circuits, is related to the supply voltage level. The main idea is to have different functions of the circuit available for different supply voltage levels (voltage ranges). At the first sight, this approach seems very promising – the supply voltage rails are connected to all gates in the circuit and there is no need for any other dedicated signals. Such gates can be used for example in applications, which must reflect a decrease or an increase of the power supply voltage by different functions in order to prevent a circuit failure caused by a lack of energy [43]. However, the range of applications where gates controlled by supply voltage level can be utilised is actually much wider.

The existing gates controlled by supply voltage level can be identified as a special type of analogue circuits which behave as digital circuits from the outside. Not all the transistors in such gates work in the saturation mode, compared to the conventional CMOS gates [72]. The gates must contain some part sensitive to the supply voltage level. With regards to the requirements for small dimensions of polymorphic gates, such part usually consists of few transistors working in a linear mode.

If a polymorphic gate can perform two (or more) different functions, then its design must be able to change the output value for certain input combinations when the power supply level changes. Let's show it on a NAND/NOR gate: When the gate inputs are different (0 1 or 1 0), the gate should deliver logic zero output value in case of NOR function and logic one for the NAND function. In order to keep the transistor count low, in several gates, the output value is ensured by more transistors opened at the same time, which deliver different logic values (both zero and one at the same time!) to the output. The resulting output voltage is then given by a ratio of channels conductivity of the opened transistors.

Besides the transistors working in a linear mode, different sizes of transistors are thus also typical for polymorphic gates controlled by supply voltage level. Such gates can contain less transistors than it would be needed for a separate (parallel) implementation of its functions. Although the transistor count seems promising, usage of transistors with different channel sizes can lead to larger layout of the gate (compare e.g. Figure 2.2b and Figure 2.2c). Mentioned switching of both logic zero and logic one to the output at the same time results in longer switching time and static current between the power rails for some gate inputs – power consumption of such gates can be then relatively high.

Table 2.1 shows all polymorphic gates controlled by the supply voltage level and published yet. Besides the pass-logic AND/OR gate, the rest of gates (NAND/NORs) has high input impedance. The output impedance usually depends on the current gate input values.

Table 2.1: A survey of polymorphic gates controlled by supply voltage level.

Functions	Control value	Transistors count	Ref.
AND/OR	1.2/3.3 V	8	[65]
NAND/NOR	3.3/1.8 V	6	[63]
NAND/NOR	3.3/1.8 V	10	[61]
NAND/NOR	5/3.3 V	8	[45]

The NAND/NOR published in [45] has both input and output levels compatible with the CMOS standard, and signal propagation time about 80 ns. Switching of both logic zero and logic one to the output at the same time (i.e. making the power rails short) results in a static current over 120 μA for some inputs [44]. For the other gates, neither valid input voltage ranges, signal propagation time nor power consumption were published. However, higher power consumption compared to the conventional gates is expected for all of them.

Two polymorphic gates controlled by the power supply voltage level were physically produced. NAND/NOR gate published in [63] is the first one. It was implemented by the Stoica's team with use of HP 0.5 μm technology. Few years later, another NAND/NOR was designed by the team from Brno University of Technology and implemented with CMOS AMIS 0.7 μm technology [45]. The latter one (shown in Figure 2.2) is most probably the most thoroughly explored polymorphic gate ever. Although its parameters (summarised above) are not ideal and the gate is not usable for commercial purposes, experiments with it took polymorphic electronics a big step forward. It was incorporated into the reconfigurable polymorphic module called REMOMO32 [52] containing 32 configurable logic elements where each of them can behave as AND, OR, XOR or polymorphic NAND/NOR. That allowed to design and test many polymorphic applications controlled by the supply voltage level, e.g. [45, 53, 57, 58].
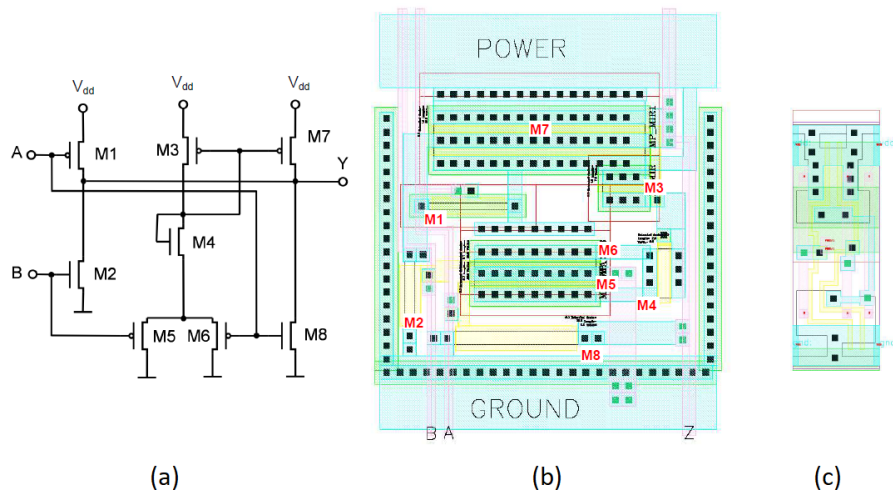
Figure 2.2: NAND/NOR gate controlled by supply voltage level [45]: (a) schematic, (b) realisation in AMIS 0.7 µm technology in comparison to (c) conventional NAND gate (4 transistors) in the same technology [44].

2.3.2 Gates controlled by chip temperature

Sensitivity of silicon semiconductor technology to the temperature of the silicon chip can also be successfully used in the design of polymorphic gates. In the conventional CMOS circuits, this sensitivity is intentionally suppressed so that the circuit performs the same function in the widest possible temperature range. However, if the circuit is designed so that the operating points of some transistors move with a change of the temperature, the circuit function may change.

The same principle is basically used also in the gates controlled by the supply voltage level, where the change of operating points occurs by changing the supply voltage. For this reason, the polymorphic circuits controlled by supply voltage level are also sensitive to the temperature and vice versa [44]. This dependence was shown on the polymorphic gate NAND/NOR from Figure 2.2 [47, 48]. If the gate was supplied by 3.3 V, at which the gate normally executes the NOR function, and the chip temperature was intentionally increased, function of the gate changed to NOT at 127 °C and then to NAND at 137 °C. When the supply voltage is higher, these temperature thresholds decrease (see Figure 2.3). There is also a certain hysteresis obvious between increasing and decreasing the temperature at a constant supply voltage in Figure 2.3.

The polymorphic gates primarily published as temperature-sensitive are listed in Table 2.2. In general, properties of those gates are rather worse. AND/OR gates published in [64] are composed of a small number of transistors with relatively small channels dimensions. However, the one with 6 transistors is a pass-logic gate with a delay up to 5 ms. The other one with 8 transistors has output levels incompatible with CMOS voltage levels: While the gate is supplied by 3.3 V, logic zero is represented by a voltage of up to 0.9 V and logic one by a voltage of down to 1.8 V at the output for certain inputs. NAND/NOR gate published in [62] is composed of 12 transistors, i.e. much more than it is needed for a separate (parallel) implementation of NAND and NOR functions. Furthermore, publication [62] provides no simulation results so it is difficult to determine other properties of the gate. NOR/NOT gate published in [70] is based on more transistors opened at the same
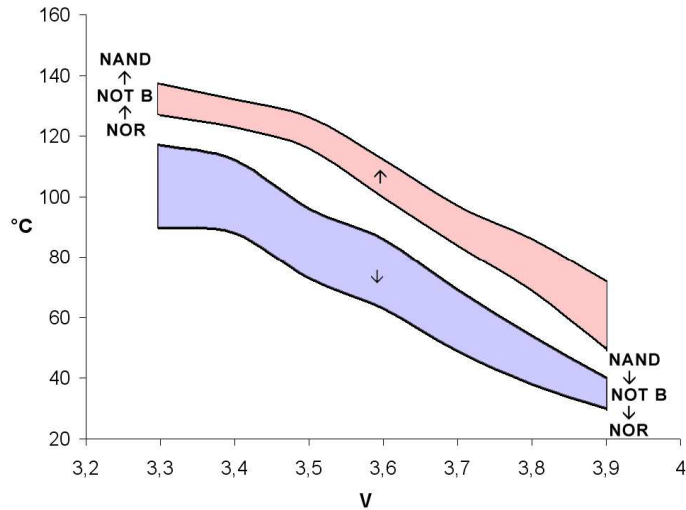
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Figure 2.3: Dependence of NAND/NOR gate from Figure 2.2 on the chip temperature and supply voltage [48].

time for some inputs. It can be predicted with a certainty that all four gates will have higher power consumption in some states (for some inputs). The remaining gates listed in Table 2.2 (AND/BUF, NAND/NOT and OR/AND) are only mentioned in [70] without any schematics. Thus, it is not possible to determine any of their parameters.

Table 2.2: A survey of polymorphic gates controlled by chip temperate.

Functions	Control value	Transistors count	Ref.
AND/BUF	25/125 °C	7	[70]
AND/OR	27/125 °C	6	[64]
AND/OR	5/90 °C	8	[64]
NAND/NOR	80/120 °C	12	[62]
NAND/NOT	25/125 °C	6	[70]
NOR/NOT	25/125 °C	6	[70]
OR/AND	25/125 °C	6	[70]

In general, the advantage of temperature-controlled polymorphic gates can be their small size and no required global signal for function change across the chip. On the other hand, the behaviour of gates controlled by a continuous physical quantity is defined only in specified intervals of this quantity. For the same input, the output of these gates may oscillate between these intervals [44]. The biggest disadvantage of temperature-controlled gates is thus a high inertia – heating and cooling of the chip is usually very slow. In addition to that, heating of the chip may not occur evenly (temperature can be different in various parts of the chip).

2.3.3 Gates controlled by dedicated control signal

Stoica's team proposed also a possibility to control the function of polymorphic gates by a dedicated control signal; more precisely by a voltage at this control wire [64]. In contrast

to the control approaches introduced above (supply voltage level and chip temperature), an additional global signal across the whole chip is required, which could make the chip more expensive.

In case of the gates implementing just two functions, the behaviour of such gates is defined only for two voltage intervals at the dedicated wire – i.e. this dedicated wire transmits a binary information similarly to any other logic signal. Thus, such gates can be understood as conventional digital circuits having one more input signal and can also be designed by conventional synthesis methods at the gate (or transistor) level. Although inclusion of such gates to the field of polymorphic electronics may be controversial, authors of polymorphic electronics consider them also as polymorphic [64]. A requirement of three (or more) functions built into a single gate leads again to an analogue design where some transistors usually work in a linear mode.

First gates, designed as configurable by a special signal, were created before the introduction of the idea of polymorphic electronics. Between 1996 and 1997, Mark W. McDermott and John E. Turner patented XNOR/XOR [26] a NAND/NOR [27] gates. The specific function was chosen through a dedicated control wire by a voltage close to zero volts or close to the power supply voltage. A specific object of the invention was to maximise the flexibility in the design of spare gate arrays, such as for use in making fixes to integrated circuits through spare gates only.

The summary of published gates controlled by a dedicated signal is shown in Table 2.3. Parameters of many of them were thoroughly investigated in [44]. They vary a lot. There is a lot of gates in which one of the input signals can be switched through transistors directly to the output, i.e. they are pass-logic: AND/OR, AND/OR/XOR, NAND/WIRE/AND and further all gates published in [66].

Table 2.3: A survey of polymorphic gates controlled by dedicated control wire.

Functions	Control value	Transistors count	Ref.
AND/OR	0/3.3 V	6	[64]
AND/OR/XOR	3.3/1.5/0 V	10	[64]
NAND/AND	3.3/0 V	? (6 or 8)	[66]
NAND/NOR	0/5 V	10	[27]
NAND/NOR	0/5 V	10	[74]
NAND/NOR	5/0 V	8	[44]
NAND/NOR	5/0 V	10	[44]
NAND/NOR/XNOR/AND	0/0.9/1.1/1.8 V	11	[75]
NAND/XOR	5/0 V	9	[42]
NAND/WIRE/AND	0/1/-1.8 V	9	[76]
NOR/AND	3.3/0 V	? (6 or 8)	[66]
OR/NAND	3.3/0 V	8	[66]
OR/NOR	3.3/0 V	8	[66]
XNOR/XOR	5/0 V	16	[26]

The most interesting gate is definitely the NAND/NOR/XNOR/AND gate which implements four different functions in a single circuit just by 11 transistors [75]. It was designed

as an analogue circuit, similarly to AND/OR/XOR and NAND/WIRE/AND gates. It can be assumed that they will all have higher power consumption.

Four polymorphic gates were published in [66]. According to the publication, proposed gates do not follow the conventional CMOS design, so their output levels are sometimes 0.5 V for logic zero and 2.5 V for logic one whereas the gates were supplied by 3.3 V. Unfortunately, image quality of schematics and graphs with simulation results is low, so the results are not reproducible. Moreover, NAND/AND and NOR/AND gates are once drawn with 6 transistors, once with 8 transistors, although just one circuit was designed for each polymorphic function.

The rest of gates (NAND/NORs, NAND/XOR, XNOR/XOR) have a high input resistance, low output resistance, and input and output levels usually in the range of CMOS circuits. Their power consumption is also most probably comparable with similar CMOS circuits (it was not simulated for many gates or the results were not published). It is worth to note that NAND/NOR gate designed by L. Stareček and depicted in Figure 2.4 was implemented using the AMIS 0.7 μm technology [44].
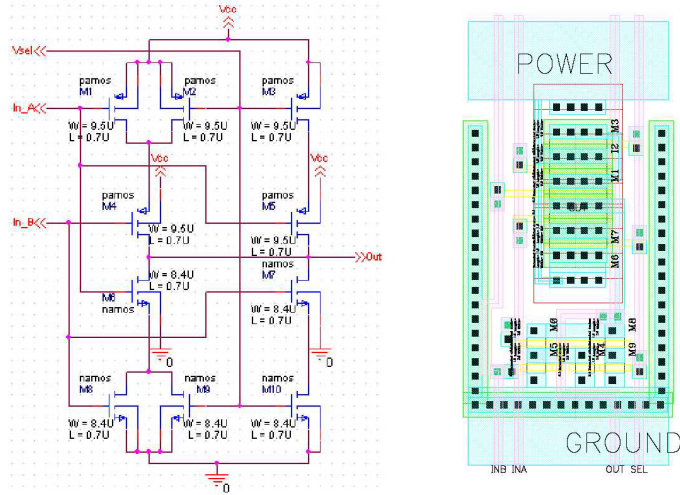

Figure 2.4: NAND/NOR gate controlled by a dedicated control input (left) and its physical realisation using AMIS 0.7 μm (right) [44].

Gajda mentioned also WIRE/OR/XOR/AND2b/NAND/AND1b polymorphic gate in his PhD thesis [17]. However, this gate was not found in the provided reference.

2.3.4 Gates controlled by supply voltage polarity

Technologies based on MOSFET and FinFET transistors are undoubtedly dominant in the today's electronics. However, they are slowly approaching the physical limitations (channel size, heat dissipation from the chip, etc.) [22, 59]. Thus, it began to search for transistors that could completely replace conventional silicon transistors in the future, or at least to find a convenient alternative. The exploitation of beyond silicon devices like carbon nanotubes (CNT) [24], graphene [39] and silicon nanowires (SiNW) [9] based transistors, as well as organic single crystal [14] or heterostructures [15], is considered by some researchers as a potential answer.

Ambipolar transistors

It has been shown in various literature sources that many post-silicon devices developed in recent years exhibit so-called ambipolar behaviour. The principle behind the ambipolar behaviour of such a transistor is that the transistor operates like N-type conventional MOS transistor under certain conditions and like P-type conventional MOS transistor under other conditions.

Ambipolar transistors have several variants. In this thesis, double-independent-gate ambipolar FETs are primarily investigated and utilised. Examples of such transistors are shown in Figure 2.5 and Figure 2.6. While the *control gate* (marked as G or CG) works in the same way as in case of the standard unipolar FETs, the *polarity gate* (PG) controls the device conduction mode (polarity; i.e. whether the transistor works as P- or N-type). Such transistors have been reported with use of emerging technologies such as carbon nanotubes [24], graphene [20] and silicon nanowires [21, 25]. Another variant of ambipolar transistors has only one gate (three terminals in total) [3, 8]. In the future, ambipolar FETs with three [16] or even more gates [2] can also be useful.
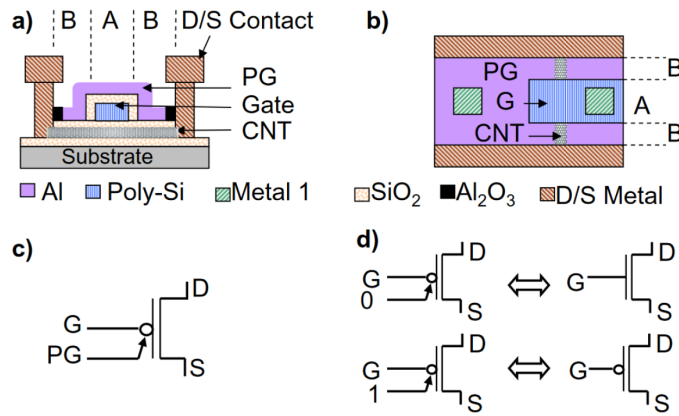

Figure 2.5: (a) Double-gate ambipolar CNT transistor, (b) layout, (c) schematic symbol and (d) a way to control its polarity in digital circuits [4].

Described behaviour of ambipolar transistors seems to be very advantageous for complementary (CMOS like) structures. Moreover, the fabrication of such circuits may be simplified – just one type of the transistor is used everywhere.

In order to reduce the number of transistors in conventional (monofunctional) circuits, a lot of gates and more complex circuits based on double-gate ambipolar transistors were designed [1, 5]. All of them were designed as conventional digital circuits with PG controlled by logic levels. The author of this thesis created a classification of double-gate transistors according to the PG terminal control which was further used in all his publications:

- **Type 1:** Ambipolar transistor acts as N-type in case of logic 1 at PG terminal and as P-type in case of logic 0 at PG terminal – e.g. CNT transistors utilised in [5] (see Figure 2.5).

- **Type 2:** Ambipolar transistor acts as P-type in case of logic 1 at PG terminal and as N-type in case of logic 0 at PG terminal – e.g. SiNW transistors utilised in [1] (see Figure 2.6).
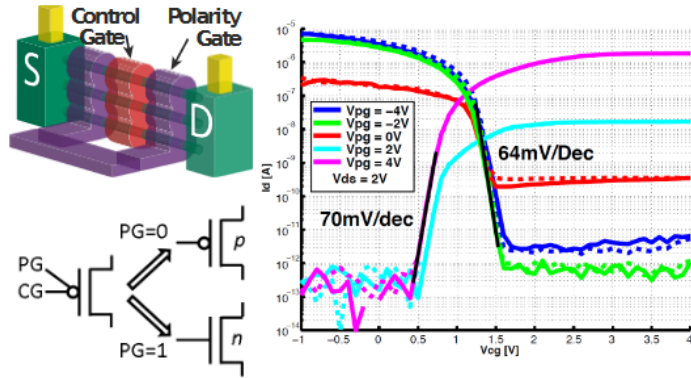
Figure 2.6: Structure of ambipolar double-gate SiNW FET, volt-ampere characteristics [25] and a way to control its polarity in digital circuits [1].

Gates controlled by supply voltage polarity

Because the polarity of ambipolar transistors is not specifically defined at an early stage by the fabrication process, but it could be changed also during the operation, it was shown that ambipolar transistors can be used with advantages also in polymorphic circuits. The idea of changing the transistor polarity by changing the logical value at PG terminal led to an idea of a new control approach for polymorphic circuits: Function of the circuit is given by the polarity of power supply rails. If such circuit is supplied for instance by five volts above ground using one supply rail and the second supply rail is grounded, the second circuit function is available when the first supply rail is grounded and the second one is supplied by five volts – i.e. when the potentials of supply rails are swapped. Based on this principle, the polymorphic circuits controlled by the polarity of supply voltage have just *two functions*.

As it is shown in paper [73], which introduced several possibilities for usage of ambipolar transistors (and which calls this type of electronics as *ambipolar electronics*), structure of such bi-functional circuits can be similar to the CMOS circuits – one part of the circuit is used for delivering of a logic one to the output (in the conventional circuits usually based on P-MOS transistors) and the other (complementary) one for delivering of a logic zero to the output (see Figure 2.7a). In a suitably designed circuit, role of these two circuit parts may mutually change by changing the supply voltage polarity.

Most of the papers introducing some new ambipolar transistor show its behaviour on an inverter, e.g. [8, 25]. The inverter consists of two transistors connected similarly to the conventional MOSFET inverter. Such inverter based on ambipolar transistors can be labelled as NOT/NOT polymorphic gate because it produces an inverted input value to the output independently of the supply voltage polarity.

Yang and Mohanram [73] show another two polymorphic gates created from double-gate ambipolar transistors – NAND/NOR and XOR/XNOR gates. The first one is based on a structure similar to the conventional implementation of NAND and NOR functions in CMOS technology (see Figure 2.7b). It utilises four transistors only. When the supply rail c_s has higher (positive) potential than $\overline{c_s}$, the gate behaves as NAND. Otherwise ($\overline{c_s}$ has higher potential than c_s), the gate performs NOR function. XOR/XNOR gate (Figure 2.7c) is also assembled from four transistors. However, it requires also inverted inputs. Thus,
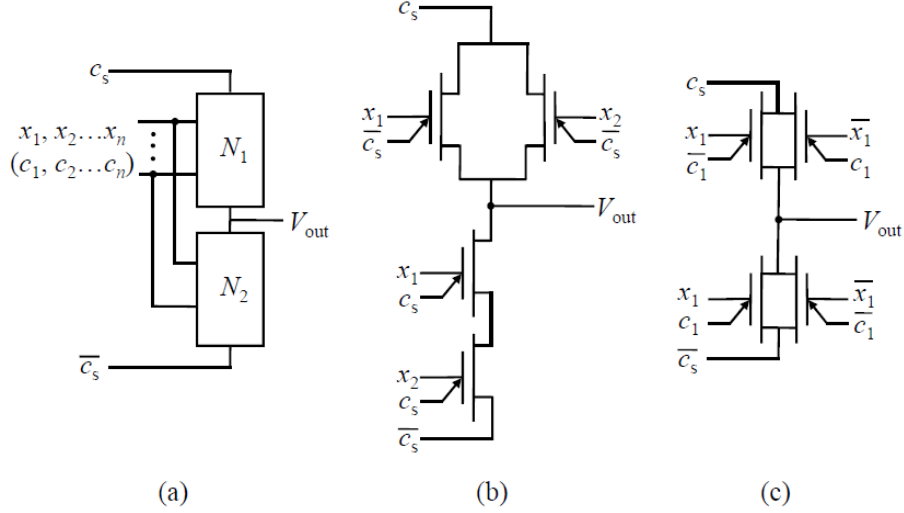
19

Figure 2.7: (a) Structure of gates controlled by power supply polarity, (b) NAND/NOR gate and (c) XOR/XNOR gate [73].

two additional inverters would be needed for its realisation and the number of ambipolar transistors would increase to eight.

All three gates (inverter, NAND/NOR and XOR/XNOR) prove to be very promising in terms of properties and criteria listed at the beginning of Chapter 2.3. High input impedance is provided by connecting of all signal inputs to the gates of transistors. Transistors operate in the saturation mode, which minimises the gate consumption. The gate output is switched from the power rails by transistors with the correct polarity. That ensures low output impedance and output voltages close to the power supply voltage. The number of transistors being used in the gates is also low. Besides inverter, which is constructed (as well as a conventional solution) from two transistors, significantly lower number of transistors were used in comparison to a separate (parallel) implementation of both functions in a conventional CMOS solution. Implementation of a potential multiplexer would further significantly increase the number of transistors in conventional solutions.

These promising parameters led the author of this thesis to the further research. As a result, a high number of polymorphic gates controlled by the polarity of power supply voltage were later designed [37, 35, 36, 38]. Different implementations of AND/OR and XOR/XNOR functions were proposed in [37] for both Type 1 and Type 2 ambipolar transistors. But what is perhaps more important than new implementations of AND/OR and XOR/XNOR functions is a fact that the used evolutionary-based circuit design method proposed by the author of this thesis earlier [34] was not able to design 32 from 36 polymorphic functions (AND/XOR, AND/XNOR, etc.).

As it is shown later in Chapter 3.2, electronics based on ambipolar transistors and supplied by two rails, which can change their potentials, is really *not functionally (Boolean-) complete*. In other words, several logic functions cannot be implemented by this type of electronics. When one or two power rails with a stable potential (v_{DD}, v_{SS}) are added to the power rails determining the circuit function, circuits can implement any logic function. Design of such circuits is shown [36]. Furthermore, it was shown that similar approach can be used also for polymorphic circuits based on MOSFET transistors [35]. Polymorphic gates designed in this way assume transistors with conventional dimensions and working

in the saturation mode. That provides much better properties (power consumption, propagation delay, size, etc.) compared to the gates controlled by supply voltage level or chip temperature (see Chapters 2.3.1 and 2.3.1).

38117 gates controlled by the polarity of dedicated supply rails were published by the author of this thesis in PoLibSi library [38], which is available at www.fit.vutbr.cz/~inevoral/polibsi. Figure 2.8 shows a screenshot from the library. The library contains eight sets of efficient bi-functional two-input polymorphic gates, whose function is selected by polarity of dedicated power rails. Particular gate sets differ in the transistor type (conventional MOSFET, double-gate ambipolar transistors), feature which the gate sets were optimised to (transistor count, propagation delay, power consumption) and input impedance constraint (see Table 2.4). Each gate implementation includes a schematic, an HSPICE description and simulation results (see Figure 4.1). The propagation delay and power consumption is provided for all MOSFET based gates. Furthermore, each gate set is complete – it provides at least one (usually even more) efficient implementation of any pair of two-input Boolean functions. That can be useful for efficient synthesis of complex polymorphic circuits.

PoLibSi Polymorphic Gate Library

Welcome

Welcome to PoLibSi, the polymorphic gate library. The library is composed of eight sets of bi-functional two-input gates. Each set usually provides more implementations of each particular polymorphic function (a pair of Boolean functions). Individual gates are defined by HSPICE descriptions and schematics. Simulation results of each gate are also a part of the library. Further details about the library are provided in [2], detais about the gate design can be found in [3-5]. Paper [1] newly investigates power consumption of MOSFET gates and introduces MOS_POWER_HI and MOS_OPT_HI gate sets.

Gate sets

- MOS_SIZE_HI gate set: MOSFET transistors, high input impedance, evolved to minimize the transistor count. Set contains different implementations of each gate while keeping the minimal number of transistors.
- MOS_DELAY_HI gate set: MOSFET transistors, high input impedance. Set contains implementations with lowest delay for different number of transistors being used in each particular gate.
- MOS_POWER_HI gate set: MOSFET transistors, high input impedance. Set contains implementations with lowest power consumption for different number of transistors being used in each particular gate.
- MOS_OPT_HI gate set: MOSFET transistors, high input impedance. Set contains implementations with lowest multiple of propagation delay and power consumption for different number of transistors being used in each particular gate.
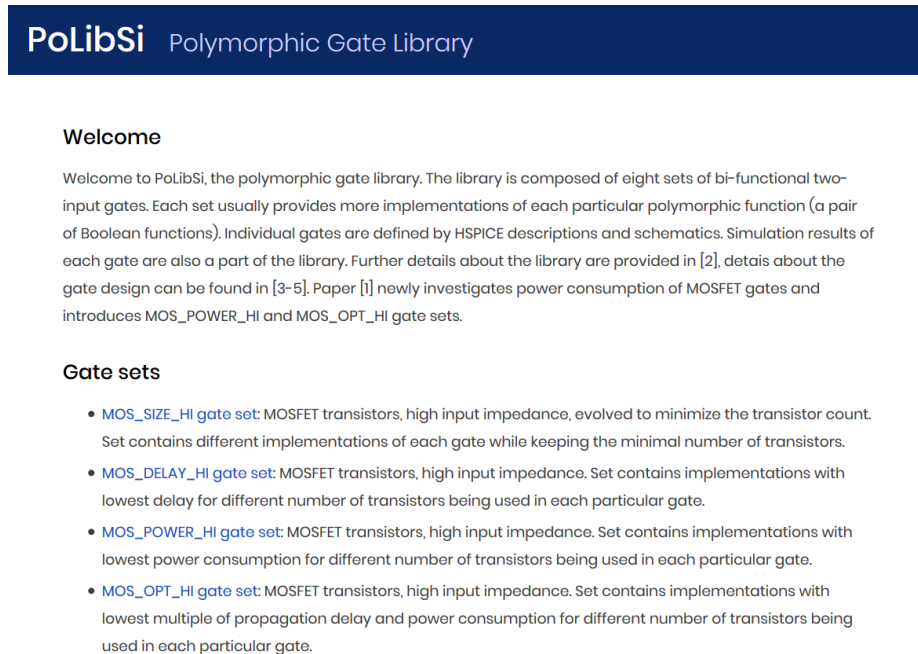
Figure 2.8: Screenshot of the PoLibSi website.

In order to make the enumeration of polymorphic circuits based on ambipolar transistors (mono-gate ambipolar transistors in this case) complete, it is also worth to mention a work of Radek Tesař. He designed two-input NAND/NAND and NOR/NOR gates resistant to the change of supply polarity [69], further identity/negation gate and a polymorphic multiplexer [68]. The last-mentioned gate propagates the first multiplexer input to its output in the first polymorphic mode and the other input in the other mode. However, these gates differ from the original concept as they use also rectifier diodes besides the ambipolar transistors.

Table 2.4: List of gate sets in the PoLibSi library.

Gate set name	Transistor type	Input impedance	Opt. criteria	No. of gates in the set
MOS_SIZE_HI	MOSFET	high	size	507
MOS_DELAY_HI	MOSFET	high	delay	257
MOS_POWER_HI	MOSFET	high	power	239
MOS_OPT_HI	MOSFET	high	delay, power	253
AMBI_N1_HI	ambipolar, type 1	high	size	11577
AMBI_N1_NO	ambipolar, type 1	–	size	4791
AMBI_P2_HI	ambipolar, type 2	high	size	11279
AMBI_P2_NO	ambipolar, type 2	–	size	9214

2.3.5 Non-conventional multifunctional gates

In the recent years, several other gates based on unconventional structures have shown to be polymorphic or at least multifunctional. This section shows three such gates.

Figure 2.9 shows a graphene-based multifunctional device whose output F is given by the relation $AC + A'B$ for $U = 1$ and $A'C + AB$ for $U = 0$ [67]. The basic function of the element is thus a multiplexer controlled by the A or U signal. If a specific constant voltage is applied to electrodes A and/or B, the gate can realise up to 8 functions derived from the mentioned formulas. However, from the viewpoint of polymorphic electronics, it is a gate with two functions. These two functions are then given by the specific connection of the gate in the circuit.
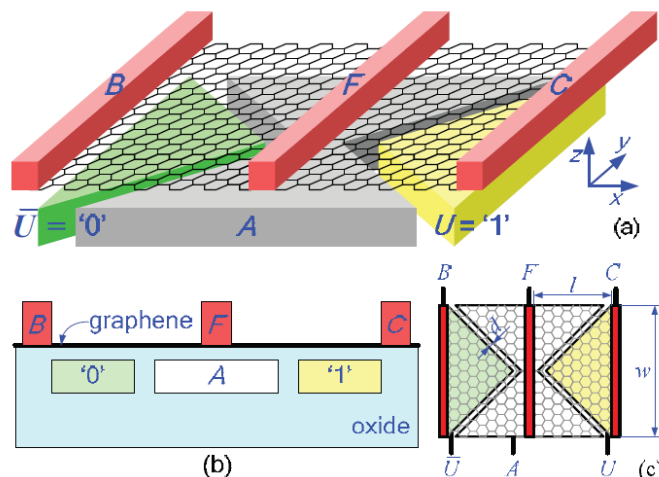

Figure 2.9: Graphene gate: (a) 3D visualisation, (b) side cut, (c) to view [67].

In 2017, Parveen's team introduced hybrid spin-CMOS logic gates using magnetic domain wall motion devices with five [41] and six terminals [40]. Their function is given by a multi-bit key (key in Figure 2.10 composes of K1, K2 and K3 signals). By applying one of the four keys, the gate can be used to implement AND, OR, identity or XOR function.

Because the gate contains also a negation of the output, functions NAND, NOR, NOT and XNOR are then also automatically available. If a suitable key signal is used as a signal describing the state of the environment, the gate could also be called as a polymorphic gate with two functions.
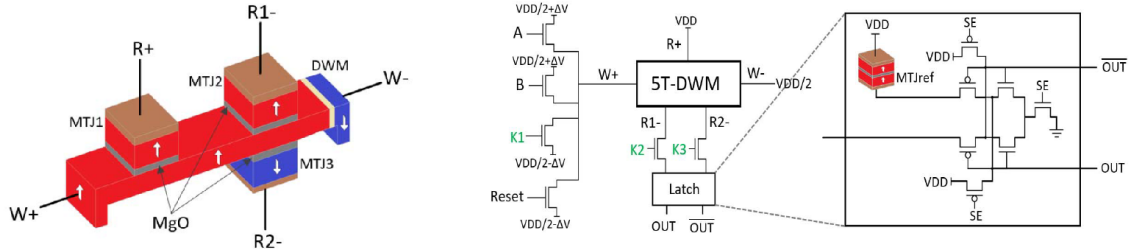

Figure 2.10: 5-terminal magnetic domain wall motion device structure (left), proposed gate (right) [41].

All three devices are multifunctional and provide implementations of different logic functions. While the graphene one could be used as a gate controlled by a dedicated control signal, the others require a complicated sequential control (reset, compute, and sense states) which is not typical for polymorphic gates. Moreover, the hybrid spin-CMOS logic gates need a high number of transistors (13 in [41] and 17 in [40]) in addition to the main domain wall motion device. That would probably not allow their deployment in the polymorphic electronics.

Chapter 3

Research summary

This chapter summarises the research presented in the thesis. After a brief overview of the research process; the motivations, contributions and abstracts for each included paper are presented. Then, other achieved results related to this thesis are summarised, which are parts of two submitted but not yet published papers. Finally, remaining papers of the author that are not included in this thesis are listed together with research projects the author participated in.

3.1   Overview

The goal of the research conducted in this doctoral thesis is to deeply investigate an approach to the gate-level polymorphism where the circuit function is selected by the polarity of supply voltage. As the basic building blocks, conventional MOSFET and emerging double-gate ambipolar transistors were chosen.

Only a few polymorphic gates controlled by the supply voltage polarity have been published earlier by other authors. Such gates were designed by an ad-hoc approach. In order to systematically design new polymorphic gates, an evolutionary-based design method was created and published in Paper I. To our best knowledge, it is the first design approach for design of circuits controlled by the supply voltage polarity and also the first approach for design of circuits based on the double-gate ambipolar transistors ever.

A subsequent research focused on the gates based on double-gate ambipolar transistors resulted in several innovative gates published in [37] and especially in the finding, that polymorphic electronics controlled by the supply voltage polarity is functionally complete only if at least one constant logic value (i.e. v_{SS} or v_{DD}) is available in the circuit. Chapter 3.2 describes the problem more in detail. In the rest of the research, it was assumed that these logic values currently exist in the circuit (polymorphic electronics is, for example, combined with conventional electronics in the chip) or it is possible to create them from the power supply rails in the particular chip manufacturing technology.

Design approach published in Paper I was later improved for a fast and reliable design for specific transistor types: Paper II is devoted to the design of polymorphic gates based on MOSFET transistors and Paper III to the design of gates based on double-gate ambipolar transistors. In both papers, complete sets of size-efficient polymorphic two-input gates are presented (five sets in total). Note that the author of this thesis is the first who came up with the idea to combine such type of gate-level polymorphism with conventional MOSFET transistors.

In order to provide the complete sets of second generation polymorphic gates to the research community, an online polymorphic gate library called PoLibSi was created (Paper IV) and released online to `www.fit.vutbr.cz/~inevoral/polibsi`. Each gate in the library includes a schematic, an HSPICE description and simulation results (see Figure 4.1). Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. Besides the size-oriented gate sets, delay-oriented, power-oriented and delay&power-oriented MOSFET gate sets were later created and attached to the library. A paper dedicated to the power consumption of the second generation of polymorphic gates is currently submitted to a conference by the author of this thesis. It was proven that properties of the designed gates are really better compared to the first generation of polymorphic gates (see Chapter 3.4). Moreover, it was shown that such polymorphic gates could be competitive to the conventional CMOS solutions in terms of the size, delay and also power consumption.

Paper V brings a case study with an intention to show on an example (adder/subtractor) that complete sets of efficient bi-functional gates may allow an efficient implementation of components at a higher level of abstraction. In several classes of applications, which typically involve RT level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level.

Chapter 3.4 shows more complex polymorphic circuits. In order to show the advantage of the proposed gate sets, bi-functional image filters were chosen as target applications. A few tens of complex size-efficient RTL components were designed and subsequently utilised for implementations of three bi-functional image filters. A part of the designed RTL components was published already in Paper IV. It was shown that designed filters are significantly smaller compared to the implementations based on the first generation of polymorphic gates. Moreover, proposed implementations are significantly smaller than conventional solutions with conventional mono-functional gates.

3.2 Problem of a constant in the environment with changing power supply polarity

In the conventional CMOS electronics, any Boolean function can be implemented only by using NAND gates or only by using NOR gates. These gates can also be utilised for implementation of unary or nullary (constants) Boolean functions. Note that the constants (logic zero and logic one) are present in the circuits by supply rails anyway.

Similarly, at least one permanent logic value (a constant) is required in the polymorphic circuits controlled by the supply voltage polarity. In 2017, author of this thesis showed that an evolutionary method for design of such polymorphic circuits was able to design only four out of 36 different two-input gates, which supposed to be based on double-gate ambipolar transistors and had no access to any permanent logic value or any other constant potential [37]. Out of all 256 possible two-input functions, only 16 were successfully designed (identity and various combinations of NOT/NOT, NAND/NOR and XOR/XNOR functions). The usage of an evolutionary algorithm cannot prove that the remaining functions cannot be designed, of course, but a proof, showing that some of the gates cannot be designed, follows:

Theorem 1 *Polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is NOT functionally (Boolean-) complete if there is no constant logic value in the circuit.*

Proof *Suppose that polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is computationally complete. Thus, for any two Boolean functions, there is a polymorphic circuit that realises them. Thus, there is also a circuit producing a permanent logic one output regardless of the supply voltage polarity (such polymorphic function can be denoted as 1/1). Let's create such a circuit.*

The logic one must be independent of any signal inputs of the circuit, because all signal input can be zero at the same time. Thus, the logic one must be switched to the output from the supply rails. In order to ensure strong (undegraded) output level, the logic one must be switched by one or more transistors with P polarity.

Let's consider the first polymorphic function of the circuit, when there is a potential corresponding to logic one at supply rail pwr0 and a potential corresponding to logic zero at supply rail pwr1. The logic one must be switched from pwr0 through one (or more) opened ambipolar transistor, currently configured to work as p-MOS. Its gate must be connected to pwr1 – to logic zero in order to ensure that the transistor will be opened (see Figure 3.1 left). The connection of PG terminal to a specific power rail (ensuring the P polarity) depends on the type of ambipolar transistor (see Chapter 2.3.4).

After swapping of supply rail potentials (i.e. changing the supply voltage polarity), a logic zero is at pwr0. Thus, at least one of the transistors mentioned above must necessarily be closed so that the logic zero from pwr0 is not propagated to the output. Since logic one is now at the gate terminal of the transistor, its polarity must remain same (p-MOS). That requires to maintain the same logic level at PG terminal as it was there before swapping of supply rail potentials (see Figure 3.1 right).

So, a constant potential is required to create a constant logic level. However, there is no constant potential in the circuit. Thus, the circuit with a permanent logic one at the output cannot be created. Thus, polymorphic electronics mentioned above is NOT functionally complete. □
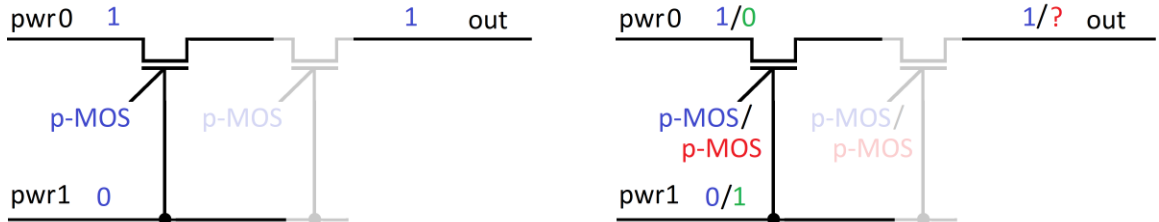

Figure 3.1: Wiring of ambipolar transistor(s) during an attempt to create a circuit generating constant logic one: Before (left) and after (right) change of supply voltage polarity.

Theorem 2 *Polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is computationally complete if at least one permanent logic value is available in the circuit.*

Proof *If just one permanent logic value is available in the circuit, the other one can be created by an inverter (NOT/NOT gate). Any polymorphic gate can then be implemented e.g. by conventional CMOS circuits realising both circuit functions, whose output is selected by a multiplexer according to one of the power supply rails. Such circuit is supplied by permanent logic one and permanent logic zero. As transistors, double-gate ambipolar transistors are used, whose PG terminal is connected either to permanent logic one or a permanent logic*

zero, depending on whether the particular transistor should behave as n-MOS or p-MOS transistor in the circuit. □

Note that the universal implementation of a polymorphic gate utilised in the proof of Theorem 2 is working for a given pair of functions, but it is most probably not the most efficient implementation of such a function.

A similar problem with constant logic values can be found also in the polymorphic circuits controlled by supply voltage polarity and based on MOSFET transistors. The substrates of n-MOS transistors are usually connected to the negative pole of the power supply and the substrates of p-MOS transistors to the positive one [72].

For the design of polymorphic gates controlled by of the supply voltage polarity, it is supposed in this thesis that the permanent logic values currently exist in the circuit (polymorphic electronics is, for example, combined with conventional electronics in the chip) or it is possible to create these permanent levels from the power supply rails in the particular chip manufacturing technology (in the MOSFET-based polymorphic electronics e.g. by PN-based rectifiers in a silicon chip).

3.3 Papers included in the thesis

This section presents details on the motivation and contributions for each paper together with the paper abstract.

3.3.1 Paper I

NEVORAL Jan, RŮŽIČKA Richard and MRÁZEK Vojtěch. **Evolutionary Design of Polymorphic Gates Using Ambipolar Transistors**. In: *2016 IEEE Symposium Series on Computational Intelligence.* Athens: Institute of Electrical and Electronics Engineers, 2016, pp. 1-8. ISBN 978-1-5090-4240-1.

Author participation: 50 %
Conference ranking: B5 (Qualis[1])

Motivation and contributions

Before 2016, no method for systematic design of gates based on ambipolar transistors nor any method for systematic design of polymorphic gates controlled by polarity of supply voltage rails was published. In this paper, we presented an evolutionary based method for design of polymorphic circuits at the transistor level. It is capable of designing both polymorphic gates controlled by the polarity of supply voltage rails and bi-functional polymorphic gates controlled by dedicated control signal. Besides double-gate ambipolar transistors, designed gates can be also based on N-MOS and P-MOS transistors.

Speed of the evolutionary based circuit design methods is mostly dependent on the speed of circuit evaluation. The proposed method is inspired by a design method published earlier by Mrázek et al. [30], because it was shown that a discrete simulator with a switch-level transistor model extended by a threshold drop degradation effect proposed originally by Mrázek is able to achieve a fast circuit simulation with a reasonable accuracy. Instead of single-output and two-input CGP nodes, we utilised single-output and three-input CGP

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[1]http://www.conferenceranks.com/

nodes which can represent ambipolar transistors, N-MOS transistors, P-MOS transistors or junctions. The evaluation of candidate circuits is performed by a discrete even-driven simulator. Six different discrete values are supported: *strong* as well as *degraded* zeros and ones, a high-impedance state and an undefined (forbidden) state. The implemented simulator generates outputs of candidate circuits for all possible input vectors and checks, whether the output values are identical with the specification, and no short-circuit connections nor any values oscillations (caused by cyclic connections) occurred during the simulation.

Two models of transistors are proposed in this paper. The first one (called *six-state*) is based on the behaviour of conventional MOSFET transistors. In the circuits designed with use of this model, degraded values at gate (and polarity gate) terminals usually have a similar impact on the transistor behaviour as non-degraded (strong) values (see Paper I, Section 4B). In this PhD thesis, the six-state model is later used for design of gates based on MOSFET transistors. The other model (called *four-state*) ensures that only non-degraded values will be present at gate (and polarity gate) terminals of utilised transistors. Because of a lack of freely available exact models of double-gate ambipolar transistors, is not possible to determine their degraded levels and also their behaviour with certainty when degraded values are present at their gates. Therefore, the *four-state* model was used for design of gates based on double-gate ambipolar transistors in the following papers.

It was demonstrated that the proposed method is able to produce valid solutions. Moreover, AND/OR and XOR/XNOR gates designed by this method provides transistor savings (i.e. size or area savings) compared to the existing polymorphic gates based on ambipolar transistors. The method proposed in this paper was further modified and utilised for design of polymorphic gate sets in attached Paper II, Paper III and Paper IV.

The proposed design method is not strictly related just to MOSFET or double-gate ambipolar transistors. If the currently implemented transistor models would correspond to behaviour of any other modern transistors (FinFET, FDSOI, etc.) or similar discrete models could be created for another types of transistors (e.g. mono-gate ambipolar transistors), the proposed design method can be easily extended by their support.

Finally, the paper introduces a new class of polymorphic gates discovered thanks to the newly proposed design method – polymorphic gates controlled by the polarity of supply voltage rails which are based purely on the conventional MOS transistors (previously published gates controlled by the same way were based on ambipolar transistors).

In this paper, a new approach suitable for the evolutionary design of smaller polymorphic circuits based on ambipolar transistors was introduced. The novelty lies in a new circuit representation and new simulation models. The approach can be utilised for design or optimisation of polymorphic circuits controlled by the polarity of supply voltage or circuits controlled by the dedicated control wire.

Abstract

The objective of the paper is to introduce a new approach to the evolutionary design of polymorphic digital circuits conducted directly at transistor level. A discrete event-driven simulator was utilised to achieve reasonable trade-off between performance and precision. The proposed approach was evaluated on a set of polymorphic logic circuits controlled by switching the power rails. It was demonstrated that the proposed method is able to produce valid solutions. A lot of polymorphic gates based on ambipolar transistors were designed, which provide transistor savings compared to existing circuits. A new class of polymorphic gates was discovered thanks to the proposed system – gates based on conventional

MOS transistors whose functions are changed by switching the power rails. They seem to have the best parameters among currently known polymorphic gates based on conventional transistors.

3.3.2 Paper II

NEVORAL Jan, RŮŽIČKA Richard and ŠIMEK Václav. **CMOS Gates with Second Function**. In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. Hong Kong: IEEE Computer Society, 2018, pp. 82-87. ISBN 978-1-5386-7099-6.

Author participation: 60 %

Conference ranking: B1 (Qualis)

Motivation and contributions

Paper I introduced a new class of polymorphic gates discovered thanks to the proposed evolutionary method – polymorphic gates controlled by the polarity of supply voltage rails which are based purely on the conventional MOS transistors. Until then, all gates controlled by the polarity of supply voltage rails were created from ambipolar transistors. In this paper, design of just such gates based on MOS transistors is investigated.

For design of new polymorphic gates, design method published in Paper I was improved in the context of this contribution. It was shown that not all the circuits produced from the method described in Paper I behave as expected (see Paper II, Figure 3). Detailed analysis of evolved circuits exposed an issue in the transistor model used in the discrete simulation, which may occur under certain conditions. In order to prevent this issue, a new design constraint (ensuring that the high-impedance discrete level will never be present at any transistor gate terminal for any circuit input) was added to the circuit requirements.

Another shortcoming of the design method proposed in Paper I turned out to be a low success rate (see Paper II, Figure 4). This issue was solved by proposing an optimisation approach based on the same design method. Furthermore, success rate was improved by reduction of the chromosome size (and thus reduction of state space) by removing one input from CGP nodes.

With such modified design approach, a set of size-efficient two-input polymorphic gates with high input impedance and controlled by dedicated power rails was created. The set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Note that it is the first complete set of polymorphic gates ever published (regardless of the control phenomenon). The gate set was later released as a part of the PoLibSi library (see Paper IV) with schematics and simulation results under name *MOS_SIZE_HI*.

The gates in the set were designed to be as small as possible (i.e. to contain as few transistors as possible). Each gate published in the set is composed of less transistors than it is required for a multiplexer and a separate implementation of individual Boolean functions. Moreover, most of the gates are also composed of same or even much smaller number of transistors than it is required for a separate (parallel) implementation of the individual Boolean functions (i.e. without multiplexer).

Gates in the set show the best parameters of all the previously published polymorphic gates: They were designed as non-pass-logic, i.e. with a high input impedance and low output impedance. All transistors work in the saturation mode. Besides the low number of transistors with conventional dimensions, the gates have also a short time of signal propagation and low power consumption compared to the first generation of polymorphic

gates. Results in this paper show that polymorphic electronics should be the concept which improves area-efficiency (price) of implementation of circuits with a second function not only at the academical level, but also in practice.

In this paper, an improved approach to the design of MOSFET-based polymorphic gates controlled by polarity of dedicated power rails was shown. Furthermore, a complete set of such two-input gates with good properties was designed and validated by HSPICE simulations. These gates bring significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size as it is shown later.

Abstract

In this paper, a new approach to design of multifunctional digital circuits is presented. It is based on adoption of polymorphic electronics paradigm which permits digital circuits to exhibit more than one function while preserving the same structure. In that case only components of the circuit (gates) have to be multifunctional. Individual gates have typically built-in sensitivity to the occurrence of some phenomena invoking the function change (e.g. power supply level etc.), which means that no dedicated net is required for that purpose. One of the key advantages of such circuits is the efficiency in terms of size. In this paper, MOS transistors are exploited in an unconventional manner where the circuit function selection depends just on the condition of power supply voltage rails, which is otherwise typical for polymorphic circuits utilising ambipolar transistors. Furthermore, a first complete set of successfully simulated two-input polymorphic gates was obtained. These gates show the best parameters of all the previously published polymorphic gates – high input impedance and low output impedance, short time of signal propagation, low power consumption and low transistor count being used. Wide range of proposed polymorphic gates (function combinations) may help to obtain more efficient results during synthesis.

3.3.3 Paper III

NEVORAL Jan, RŮŽIČKA Richard and ŠIMEK Václav. **From Ambipolarity to Multifunctionality: Novel Library of Polymorphic Gates Using Double-Gate FETs**. In: *2018 21st Euromicro Conference on Digital System Design (DSD)*. Prague: Institute of Electrical and Electronics Engineers, 2018, pp. 657-664. ISBN 978-1-5386-7376-8.

<div align="right">

Author participation: 60 %
Conference ranking: B1 (Qualis)

</div>

Motivation and contributions

As it was shown in Chapter 2.3.4, only few polymorphic gates based on ambipolar transistors were published before 2018. These gates were supplied by only two wires whose potentials were swapped when a change of the gate function was required. As it was shown in Chapter 3.2, such concept cannot create functionally complete systems. In this paper, design of gates based on double-gate ambipolar transistors with two additional power supply rails (conventional v_{SS} and v_{DD}) is investigated.

For design of new polymorphic gates, design method published in Paper I was improved in the context of this contribution. Only two types of CGP nodes are used: double-gate ambipolar transistors and junctions. Similarly to Paper II, a new design constraint was added to the circuit requirements, which ensures that the high-impedance discrete level

will never be present at any transistor gate or PG terminal for any circuit input. Because of the lack of freely available exact models of double-gate ambipolar transistors, four-state model introduced in Paper I was utilised. That ensures only strong zero or strong one discrete level to be present at any transistor gate and PG terminal for any circuit input. In order to improve the success rate of the design approach, an optimisation approach based on the same design method was proposed.

With such modified design approach, four complete sets of size-efficient two-input polymorphic gates controlled by dedicated power rails were created. Two gate sets are based on Type 1 double-gate ambipolar transistors, another two on Type 2 transistors. For each type of transistors, one set contains gates with a high input impedance and low output impedance; the other set had no impedance requirements during its design – i.e. most of the contained gates are pass-logic. Pass-logic gates are usually smaller. That can be useful in some parts of complex circuits, where pass-logic gates are also acceptable. All four sets are complete – each provides efficient implementation of any pair of two-input Boolean functions. Designed gate sets were later released as a part of the PoLibSi library (see Paper IV) under names *AMBI_N1_HI*, *AMBI_N1_NO*, *AMBI_P2_HI* and *AMBI_P2_NO*.

All gates in the sets were designed to be as small as possible (i.e. to contain as few transistors as possible). Each gate published in the sets is composed of equal or less transistors than it is required for a multiplexer and a separate (parallel) implementation of individual Boolean functions. Moreover, most of the gates are also composed of equal or even less transistors than it is required for a separate implementation of individual Boolean functions (i.e. without multiplexer). A significant difference between sizes of Type 1 and Type 2 gates can be observed – gates with a high input impedance based on Type 1 transistors are composed of approximately 1.5 more transistors in average compared to Type 2 gates.

Gates in the sets with a high input impedance (AMBI_N1_HI and AMBI_P2_HI) show the best parameters of all the previously published polymorphic gates: High input impedance, low output impedance and low number of transistors with conventional dimensions. Furthermore, short time of signal propagation and low power consumption is also expected, compared to the polymorphic gates controlled by an analogue quantity. Thus, properties of the gates should correspond to the ideal ones defines in Chapter 2.3.

In this paper, an improved approach to the design of polymorphic gates based on double-gate ambipolar transistors and controlled by polarity of dedicated power rails was shown. Furthermore, four complete sets of such two-input gates with good properties were designed and validated by HSPICE simulations. These gates bring significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size as it is shown later.

Abstract

Ambipolarity, a unique feature typically found in some beyond silicon devices, e.g. CNT or organic FETs, is still treated today just as something rather peculiar. But in reality, it does not hinder such devices from utilisation when it comes to the implementation of logic. From other point of view, this feature could be perceived as an opportunity to implement the logic in more refined and efficient way. The practical impact of ambipolarity results in devices which becomes more versatile than conventional FET element. In this paper, a set of multifunctional logic gates based on ambipolar FETs is presented. The multifunctionality of these gates means that each gate could exhibit one of two defined functions in a given moment. The selection of their function depends on circumstances under which the circuit is operated. The proposed set of gates could be employed in multifunctional circuits using

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techniques and procedures established for polymorphic electronics. This field of study, yet proposed nearly 20 years ago, now offers synthesis methods and application approaches to obtain an efficient implementation of more than one function in one logic circuit.

3.3.4 Paper IV

NEVORAL Jan, ŠIMEK Václav and RŮŽIČKA Richard. **PoLibSi: Path Towards Intrinsically Reconfigurable Components**. In: *2019 22nd Euromicro Conference on Digital System Design (DSD)*, Kallithea, Chalkidiki: Institute of Electrical and Electronics Engineers, 2019, pp. 328-334, ISBN 978-1-7281-2861-0.

<div align="right">

Author participation: 70 %

Conference ranking: B1 (Qualis)

</div>

Motivation and contributions

The main intention of Paper II and Paper III was to show how to design size-efficient polymorphic gates based on MOSFET and double-gate ambipolar transistors. It was also shown that it is possible to design such gates with a relatively small number of transistors. The main goal of this paper is to introduce a library, which contains specific implementations of such gates. The library is called PoLibSi and it is freely available for the research community at `www.fit.vutbr.cz/~inevoral/polibsi`.

The PoLibSi library is composed of eight sets of gates controlled by the polarity of dedicated power rails. Four of them are based on double-gate ambipolar transistors, another four on MOSFET transistors (see Table 2.4). Besides the size-oriented MOSFET gate set, delay-, power- and delay&power-oriented MOSFET gate sets are also part of the library.

During development of the PoLibSi library, more than ten thousand of fully operational variants of MOSFET-based gates were obtained for each particular polymorphic function. Of course, it was not an exception to observe different level of mutual similarity between some of them. However, a plenty of implementations were still completely unique and did not share any structural similarity. That particular fact has allowed to create also delay-oriented, power-oriented and delay&power-oriented MOSFET gate sets. Although only size-oriented and delay-oriented sets were finished at the time of writing Paper IV, the library currently contains all eight sets. A paper dedicated to power consumption of polymorphic gates was submitted to a different conference by the author of this thesis later (see Chapter 3.4).

Each gate set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Furthermore, each polymorphic function (a pair of Boolean functions) in the gate sets usually has more unique transistor-level implementations contained in the PoLibSi, not just a single one.

The PoLibSi library is composed of 38117 polymorphic gates in total. Each of them was simulated in order to validate its function: MOSFET-based gates by 45nm transistor models; gates based on ambipolar transistors using a behavioural model of such transistors (see Paper IV, Figure 3). The author of this thesis later proved that the MOSFET-based gates are functional also with 32nm and 65nm transistor nodes (see Chapter 3.4).

Each gate in the library includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. It turned out that the size-optimised MOSFET gates usually have little bit higher power consumption and longer propagation delay (compared to the conventional

CMOS logic gates, but still much better compared to the first generation of polymorphic gates). Th Power consumption and the delay of those gates with few more transistors (e.g. gates from the delay&power-oriented gate set) is significantly lower. Such polymorphic gates could be then competitive to the conventional CMOS solutions in terms of the size, the delay and also the power consumption! Unfortunately, a lack of freely available accurate SPICE-based models of double-gate ambipolar transistors has not allowed to investigate the propagation delay and power consumption for gates based on double-gate ambipolar transistors.

A size-efficiency of the proposed size-oriented gate sets is demonstrated by three RTL components in this paper. Their implementation is significantly smaller compared to the previous implementation from Sekanina et al. [54], who used a combination of conventional mono-functional gates and a polymorphic NAND/NOR gate – so far typical approach for polymorphic circuits.

In this paper, a large library of polymorphic gates with promising parameters is presented. It is the first freely available library with polymorphic gates ever. Each gate implementation includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. Besides the size-oriented gate sets, delay-, power- and delay&power-oriented sets dedicated to the MOSFET transistors are also part of the library. It is supposed that the proposed library may significantly improve complex polymorphic circuits in terms of the resulting size, the delay and/or the power consumption. Compared to a few dozen gates of the first generation, author of this thesis also showed that the problem with a lack of polymorphic gates offering good properties is well solvable.

Abstract

One of the main research directions of polymorphic electronics is focused on various issues connected with the design of basic polymorphic components – polymorphic gates. Without a sufficient amount of polymorphic gates offering good properties, conventional electronics will be most likely the preferred way to polymorphic electronics in application scenarios targeting multifunctional behaviour or reconfiguration. The main objective of this paper is to propose a library called PoLibSi which contains eight sets of efficient bi-functional two-input polymorphic gates, whose function is selected by mutual polarity of dedicated power rails. The gate sets differ in the transistor type (conventional MOSFET, emerging double-gate ambipolar transistors), feature the gate sets were optimised to (transistor count, delay, power consumption) and input impedance constraint. The individual gates were designed by means of using an evolutionary based approach and further validated by HSPICE simulations. Each gate implementation includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET based gates. Furthermore, each gate set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Besides providing polymorphic gates with better properties to the research society, the aim of the proposed library is to improve the synthesis of polymorphic circuits in terms of the resulting size, as it is also shown in the paper. Finally, the PoLibSi library is available at: `www.fit.vutbr.cz/~inevoral/polibsi`.

3.3.5 Paper V

Author participation: 75 %

Motivation and contributions

As it has been already stated in Chapter 2.2, logic synthesis of polymorphic digital circuits is very challenging. Most of the existing circuits were created using evolutionary algorithms.

In this paper, a case study is presented showing that it is possible to effectively implement bi-functional RTL components when a complete set of efficient bi-functional gates is available. In applications involving design at the RT level (e.g. signal processing), multifunctional RTL components could circumvent issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at the RT level a skilled designer would be still able to design far more complex circuits only by himself.

A demonstration of this assumption is given by a bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/subtractor circuit was created and optimised. It was subsequently utilised for design of multi-bit adder/subtractor. Three-bit adder/subtractor was then implemented by the size-efficient MOSFET-based gate set from Paper II and successfully simulated at the transistor level. Besides adder/subtractor, an increment/decrement RTL component is also presented. More complex RTL components were designed later by the author of this thesis. Their summary can be found in Chapter 3.4.

This paper demonstrates on an example that complete sets of efficient polymorphic gates can contribute to efficient implementations of RTL components. Such components could then move the synthesis of polymorphic circuits one level up – to the RT level. Furthermore, new circuits (new in the field of polymorphic electronics) are presented: increment/decrement, adder/subtractor.

Abstract

The emergence of highly optimised implementations of many bi-functional gates allows an efficient implementation of components at a higher level of abstraction. In several classes of applications, which typically involve RT-level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at RT level a skilled designer is still able to design far more complex circuits by himself. If a set of efficient bifunctional RTL components is available, their utilisation is expected to improve efficiency of the resulting circuit. In this paper, validity of this assumption is demonstrated through a design of bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/subtractor circuit was created and optimised. This circuit was subsequently utilised for design of multi-bit adder/subtractor which was successfully simulated at the transistor level with MOSFET implementation of bi-functional logic gates. Besides adder/subtractor, an increment/decrement RTL component is also presented.

3.3.6 Author's contributions to selected papers

The papers presented in this PhD thesis arose mainly as a part of research of the Unconventional Digital Circuits Research Group at Faculty of Information Technology, Brno University of Technology. The evolution approach presented in the first paper was inspired by an idea published earlier by Vojtěch Mrázek (also Faculty of Information Technology, BUT) who provided a lot of valuable advice and also participated in preparation of the first paper. Although all co-authors contribute to the selected papers, author of this thesis has the main share in all of them, especially in terms of the presented results. The following list summarise author's contribution to the selected papers:

1. **Paper I** – Novel circuit representation, discrete models of ambipolar transistors, implementation of the evolutionary algorithm and experimental evaluation.

2. **Paper II** – Approach to the design of gates based on MOSFET transistors, development of size-efficient gate set, validation of functionality of the gates.

3. **Paper III** – Approach to the design of gates based on double-gate ambipolar transistors, development of size-efficient gate sets, validation of functionality of the gates.

4. **Paper IV** – Development of whole PoLibSi library which primarily included: Development of the gate sets, validation of functionality of the gates, analysis of propagation delay and power consumption, creation of HSPICE descriptions, schematics and library front-end.

5. **Paper V** – Development of presented gate-level circuits and their validation, proof of the concept by a case-study.

3.4 Following results

Author of this thesis continued with the research related to the second generation of polymorphic gates also after submission of the presented papers. This section briefly summarises the results of two more submitted but in the time of writing this thesis not yet published papers.

3.4.1 Power consumption of proposed gates

In order to get a better insight to properties of the gates from the PoLibSi library, power consumption of the proposed gates was investigated by the author of this thesis. Average power consumption was calculated with use of the HSPICE simulator and added into the library for each MOSFET-based gate set. Furthermore, a huge amount of function implementations produced by the evolutionary based design approach allowed to create two novel power-oriented MOSFET-based gate sets and to attach them to the PoLibSi library:

- **MOS_POWER_HI** – contains gates with the lowest power consumption for different number of transistors being used.

- **MOS_OPT_HI** – contains gates with the lowest multiple of delay and power consumption for different number of transistors being used.

All MOSFET-based gate sets in the PoLibSi library were validated with 45nm BSIM4 V1.0 models from [31] during their design. Besides the experiments carried out with 45nm transistor model, further analysis with 32nm and 65nm BSIM4 V1.0 models from [31] was also done. In this case, the main goal was primarily to validate the fact whether the same gates exhibit stable operation also with different transistor technology nodes. Moreover, the attention was also given to the fact if the properties of the most power efficient gate would be independent of the actual transistor model.

Concerning the actual simulation runs, recommended supply voltages [80] together with sizes of transistors directly proportional to the selected technology were chosen. The measurement results for NOR/XNOR gates can be found in Table 3.1. It has been successfully confirmed that the gates are functional also when using 32nm and 65nm technologies. Moreover, the best gates (best in terms of the propagation delay and/or the power consumption) simulated using 45nm models mostly turned out to be dominating also with the other types of transistor models previously mentioned.

Table 3.1: Propagation delay and power consumption of NAND/NOR gates from the PoLibSi library in 32nm, 45nm and 65nm transistor technology nodes.

Function			65nm, 1.1V		45nm, 1.0V		32nm, 0.9V	
(Gate set)	ID	Trans.	Delay [ps]	Pwr [nW]	Delay [ps]	Pwr [nW]	Delay [ps]	Pwr [nW]
NOR/XNOR (MOS_SIZE_HI)	b1026	7	68	2203	93	1199	107	694
	b1030	7	93	3410	132	1746	150	1029
	b1060	7	93	3354	131	1727	152	1012
	b1499	7	67	2158	91	1174	105	682
NOR/XNOR (MOS_DELAY_HI)	b1499	7	67	2158	91	1174	105	682
	b371	9	55	2246	60	1030	74	658
	c906	10	51	2853	52	1485	59	823
	k412	11	27	835	26	434	27	245
NOR/XNOR (MOS_POWER_HI)	b1499	7	67	2158	91	1174	105	682
	a296	8	90	2001	130	1081	176	598
	b371	9	55	2246	60	1030	74	658
	a552	10	58	898	72	440	111	259
	j658	11	43	719	43	368	44	202
NOR/XNOR (MOS_OPT_HI)	b1499	7	67	2158	91	1174	105	682
	b371	9	55	2246	60	1030	74	658
	g100	10	58	910	65	446	85	262
	k412	11	27	835	26	434	27	245

At this point, the following consideration is naturally arising. How good do the MOSFET based polymorphic gates released in the PoLibSi library prove to be in a direct comparison to circuits implemented by means of using conventional approaches? Are the novel polymorphic gates competitive in terms of the number of transistors, the power consumption and the propagation delay? In general, positive answer can be obviously concluded for gates from the *MOS_OPT_HI* gate set, which is optimised to all those criteria.

As an illustrative example, NOR/XNOR gate was chosen – specifically its implementation with identifier k412 (11 transistors, 26 ps, 434 nW, see Table 3.1). HSPICE simulations of the conventional NOR and XNOR gates with the same transistor models clearly showed interesting evidence that separate (parallel) implementations of NOR and XNOR functions

achieved higher transistor count (12 vs. 11) and demands more power in total (475 nW vs. 434 nW) compared to #k412 NOR/XNOR gate, while the propagation delay is similar (≈ 27 ps). Moreover, the advantage of polymorphic NOR/XNOR gate can be recognised in the already implemented switch between these NOR and XNOR functions, which comes as a natural built-in feature of such circuit components. An implementation of such a switch by means of utilising dedicated piece of additional circuitry would render the conventional circuit to score much worse in all the compared properties.

Another example could be given by means of analysing $0/b$ gate (ID: i1033, 5 tr., 19 ps, 180 nW). Its output assumes a permanent logic 0 in the first mode and an identity of the input in the other mode. For a separate implementation of these functions, no transistor is needed. However, when you consider that the gate is multifunctional and, moreover, it has a high input impedance, then the gate is definitely competitive to the conventional solutions. It should be also emphasised that just a pass-transistor implementation of a single multiplexer requires 6 transistors, power consumption of 233 nW and brings 16 ps delay. Similarly, other gates from the from the MOS_OPT_HI gate set can be identified as comparable or even better.

It was shown that the second generation of MOSFET-based polymorphic gates has much better parameters compared to the first generation. Furthermore, in general, the size-optimized MOSFET gates from the PoLibSi library usually tend to exhibit higher power consumption and longer propagation delay (among the gates of the second generation). By using a few more transistors in the gates, their power consumption and their delay can be improved towards significantly lower values as power&delay-oriented gate set shows. Such polymorphic gates then become competitive to the existing conventional solutions. Thus, polymorphic electronics could be now a reasonable alternative for a designer when a circuit with a second (alternative) function is needed.

3.4.2 Applications of proposed gates

In order to show the advantage of the proposed gate sets, bi-functional image filters were chosen as target applications. To implement these filters as polymorphic circuits, more than twenty size-efficient 8-bit polymorphic RTL components were designed. As target technologies, all previously discussed transistor types were chosen: Ambipolar transistors of Type 1 and Type 2 as well as MOSFET transistors. More precisely, size-efficient gate sets with a high input impedance out of the PoLibSi library were utilised: MOS_SIZE_HI, AMBI_N1_HI, AMBI_P2_HI. Chosen bi-functional RTL components were designed for each transistor type separately.

Table 3.2 shows the resulting number of gates and transistors of the designed RTL components. Implementations of some of them were previously published also by Sekanina et al. [54], who implemented them with a combination of conventional (mono-functional) gates and polymorphic NAND/NOR gate, so far typical approach to implementation of polymorphic circuits. Sekanina designed the components with respect to *relative implementation cost* (relative area). In order to approximately compare the relative cost of Sekanina's components with the newly designed components, whose size is determined in number of transistors, a ratio of 1:4 (4 transistors match one area unit) was considered. That keeps 1 area unit cost of NAND and NOR gates, which are implemented same or similar in all compared technologies.

Calculated relative area and area saving compared to Sekanina's components is listed in Table 3.2 for each RTL component. Relative area of designed RTL components is up

Table 3.2: Implementation cost of RTL components published in [54] and implementation cost of RTL components designed with use of the gate sets from the PoLibSi library. Columns with approximate area savings are denoted „Save".

RTL component	[54] Gates	[54] Area	MOS_SIZE_HI Trans.	Gates	Area	Save [%]	AMBI_N1_HI Trans.	Gates	Area	Save [%]	AMBI_P2_HI Trans.	Gates	Area	Save [%]
or/add			170	34	42.5		208	34	52.0		191	34	47.8	
or/adds	78	93.8	211	45	52.8	43.8	255	45	63.8	32.0	230	45	57.5	38.7
adds/id			239	50	59.8		286	52	71.5		232	48	58.0	
and			48	8	12.0		48	8	12.0		32	8	8.0	
id/add	69	88.1	182	37	45.5	48.4	216	37	54.0	38.7	182	36	45.5	48.4
id/min	50	68.3	203	51	50.8	25.7	234	51	58.5	14.3	204	51	51.0	25.3
max/add	114	139.2	344	79	86.0	38.2	404	85	101.0	27.4	348	79	87.0	37.5
max/adds			366	83	91.5		442	93	110.5		390	92	97.5	
max/div2	83	98.9	246	58	61.5	37.8	288	59	72.0	27.2	244	58	61.0	38.3
max			204	52	51.0		232	52	58.0		202	51	50.5	
mean/max	118	135.9	330	73	82.5	39.3	368	68	92.0	32.3	308	68	77.0	43.3
min/max	74	86.3	224	52	56.0	35.1	230	53	57.5	33.4	202	51	50.5	41.5
min/mean	117	144.9	346	80	86.5	40.3	407	86	101.8	29.8	360	82	90.0	37.9
min			202	51	50.5		228	53	57.0		202	51	50.5	
min/or			220	51	55.0		232	53	58.0		202	51	50.5	
nand/and	18	26.1	56	8	14.0	46.4	64	8	16.0	38.7	64	8	16.0	38.7
nand/min	77	100.0	218	51	54.5	45.5	267	52	66.8	33.3	227	51	56.8	43.3
or/max	64	90.3	216	50	54.0	40.2	230	52	57.5	36.3	200	50	50.0	44.6
xnor/mean	78	97.8	199	40	49.8	49.1	247	43	61.8	36.9	214	44	53.5	45.3
xor/inv	18	25.5	56	8	14.0	45.1	72	8	18.0	29.4	64	8	16.0	37.3
xor/mean	64	83.0	202	40	50.5	39.2	248	43	62.0	25.3	208	41	52.0	37.3
Average	73.0	91.3	213.4	47.7	53.4	41.0	247.9	49.3	62.0	31.1	214.6	48.0	53.6	39.8

to 49% lower (41% in average) in case of MOSFET transistors, up to 39% lower (31% in average) in case of type 1 ambipolar transistors and up to 48% lower (40% in average) in case of type 2 ambipolar transistors. Although the mentioned ratio is approximate only, it is obvious that the implementation cost of newly designed components is significantly lower. That confirms a hypothesis that a design based on complete sets (complete in terms of the gate functionality) of efficient polymorphic gates of the second generation is more efficient than a design based on a combination of conventional mono-functional gates and a single bi-functional gate (NAND/NOR).

Designed polymorphic RTL components were subsequently used for implementation of three bi-functional image filters. These filters were proposed in [54] for image filtering of various types of noise (shot noise and Gaussian noise elimination), edge detection, dilatation and erosion. The filters are considered as digital circuits with nine 8-bit inputs (3x3-pixel kernel) and one 8-bit output, which process grayscale (8-bits/pixel) images. Their filtering abilities are comparable to the conventional solutions while the implementation cost is significantly lower [54].

Table 3.3 compares implementation costs (relative area) of the filters when different sets of RTL components are utilised. Column „CoABC [54]" shows cost of filters whose RTL components were implemented with conventional mono-functional gates and later optimised by ABC [6]. Mode of such RTL components, and thus also mode of the filters, is selected by a dedicated input wire (i.e. additional circuit input).

Table 3.3: Implementation cost of image filters created by different RTL components. Ratio of the cost of the newly proposed implementations against column „Proposed in [54]" (implementations with combination of NAND/NOR gates and conventional gates) is expressed in brackets.

Image filter	CoABC [54]	Proposed in [54]	MOSFET	Amb. Type 1	Amb. Type 2
Dilatatation/Erosion	569	659	441 (67%)	461 (70%)	404 (61%)
Edges/Shots	1089	1156	743 (64%)	834 (72%)	724 (63%)
Gauss/Shots	1639	1735	1114 (64%)	1290 (74%)	1118 (64%)

The following column in Table 3.3 (column „Proposed in [54]") represents filters based on the RTL components already mentioned in Table 3.2 – i.e. RTL components created with a combination of conventional (mono-functional) gates and polymorphic NAND/NOR gates and optimised by CGP. Implementation cost of such filters is higher than the conventional one. According to the authors of these filters, it is caused by a high implementation cost of polymorphic multiplexers (6.67 area units) [54].

The second generation of polymorphic circuits brings efficient implementation of the polymorphic multiplexer. Its relative cost is 1.5 in case of MOSFET gate set and 2.0 in case of double-gate ambipolar transistors [32]. However, the low cost of newly designed RTL components is primarily given by a high amount of efficient gates, not only by efficient implementation of the multiplexer!

Last three columns of Table 3.3 show the relative costs of filters created out of the newly designed RTL components – components with the same functions but implemented by polymorphic gates from the PoLibSi library. Implementation costs of those filters are lower compared to the filters where only NAND/NOR gates and conventional gates are con-

sidered (implementation cost ratio is stated in Table 3.3 in brackets). Moreover, proposed implementations are also more size-efficient than filters designed by conventional gates and conventional design approaches (CoABC column). Note that the image filtering capabilities remain exactly the same.

3.5 List of other publications

2017

- ŠIMEK Václav, NEVORAL Jan, CRHA Adam and RŮŽIČKA Richard. **Towards Design Flow for Space-Efficient Implementation of Polymorphic Circuits Based on Ambipolar Components.**. In: *ElectroScope*. Plzeň: University of West Bohemia in Pilsen, 2017, vol. 11, no. 1, pp. 1-10. ISSN 1802-4564.

  Author participation: 20 %

- NEVORAL Jan, ŠIMEK Václav and RŮŽIČKA Richard. **Compact Library of Efficient Polymorphic Gates based on Ambipolar Transistors**. In: *2017 12th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*. Palma de Mallorca: IEEE Circuits and Systems Society, 2017, pp. 155-160. ISBN 978-1-5090-6376-5.

  Author participation: 65 %

2016

- NEVORAL Jan. **Polymorfní obvody na bázi ambipolárních tranzistorů**. In: *Počítačové architektury a diagnostika PAD 2016*. Bořetice: Faculty of Information Technology BUT, 2016, pp. 45-48. ISBN 978-80-214-5376-0.

  Author participation: 100 %

3.6 Research projects and grants

- FIT-S-17-3994 – *Advanced parallel and embedded computer systems, Brno University of Technology*. Team member.

- LD14055 – *Unconventional Design Techniques for Intrinsic Reconfiguration of Digital Circuits: From Materials to Implementation, Ministry of Education, Youth and Sports Czech Republic*. Team member.

- FIT-S-14-2297 – *Architecture of parallel and embedded computer systems, Brno University of Technology*. Team member.

Chapter 4

Conclusions

This chapter summarises the results presented in this thesis and gives conclusions and possible directions for future work.

One of the main issues behind the adoption of polymorphic electronics is related to the lack of suitable polymorphic components – polymorphic gates. Although there have been published more than twenty polymorphic gates controlled by the supply voltage level, the chip temperature or the dedicated control signal, parameters of most of them are far from the ideal ones; no matter whether the power consumption, speed (propagation delay) or area occupied in the chip is taken into account.

The main goal of the research conducted in this thesis was to deeply investigate an approach to the gate-level polymorphism where the circuit function depends on the polarity of supply voltage. It was assumed that a discrete control quantity of such gates can simplify their design and significantly improve their properties compared to the previously published gates (gates of the first generation).

4.1   Contributions

Only a few polymorphic gates controlled by the supply voltage polarity have been published earlier by other authors. Such gates were designed by an ad-hoc approach. In order to systematically design new polymorphic gates at the transistor level, an evolutionary-based design approach was proposed and further improved for design purposes of circuits based on conventional MOSFET and emerging double-gate ambipolar transistors. Fast and sufficiently accurate evaluation of the candidate solutions was reached by discrete simulation with a switch-level transistor model extended by a threshold drop degradation effect. The novelty of the proposed design approach lies primarily in a new circuit representation and new simulation models of transistors. It was shown that the proposed method is successfully capable of designing size-efficient polymorphic gates and smaller polymorphic circuits controlled by the supply voltage polarity. To our best knowledge, it is the first approach for design of circuits controlled by the supply voltage polarity ever and also the first approach for design of circuits based on double-gate ambipolar transistors ever.

It was shown that polymorphic electronics controlled by the supply voltage polarity is not functionally complete when no constant logic value is available in the circuit. In the rest of the research, it was assumed that logic constants (logic zero and logic one) currently exist in the circuit (polymorphic electronics is, for example, combined with conventional

electronics in the chip) or it is possible to create them from the power supply rails in the particular chip manufacturing technology.

Using the evolutionary method, five complete sets of size-efficient bi-functional two-input polymorphic gates controlled by the polarity of dedicated supply voltage were designed. One set is based on MOSFET transistors, the others on double-gate ambipolar transistors. These sets were exposed to the research community in a freely available online library called PoLibSi. Each gate published in the sets is composed of less transistors than it is required for a multiplexer and a separate implementation of individual Boolean functions. That confirmed the hypothesis formulated in Chapter 1.3 of this thesis. Moreover, most of the gates are also composed of same or even much smaller number transistors than it is required for a separate implementation of the individual Boolean functions (without multiplexer).

All gates were validated by HSPICE simulator for 32, 45 and 65nm technology nodes. Furthermore, the delay and the power consumption of all MOSFET gates from the PoLibSi library were determined and attached to the library together with delay-, power- and delay&power-oriented MOSFET-based gate sets. It was shown that the parameters of the MOSFET-based gates are significantly better compared to the first generation of polymorphic gates. Moreover, gates from the delay&power-oriented MOSFET-based gate set proved to be competitive to the conventional solutions in terms of the size, propagation delay and also the power consumption. Accurate properties of the gates based on double-gate ambipolar transistors were unfortunately not investigated because of a current lack of freely available accurate SPICE-compatible transistor models.

All gate sets in the PoLibSi library are complete, i.e. each provides efficient implementation of any pair of two-input Boolean functions. It is supposed that the proposed library may significantly improve complex polymorphic circuits in terms of the resulting size, delay and/or the power consumption. Compared to a few dozen gates of the first generation, author of this thesis showed that the problem with a lack of polymorphic gates with good properties is well solvable (PoLibSi contains even 38117 gates).

Furthermore, it was demonstrated that complete sets of efficient polymorphic gates can contribute to size-efficient implementations of more complex polymorphic circuits. Case study with bi-functional RTL components and applications with two functions were presented. Newly designed RTL components were 14.3 – 49.1% (37.1% in average) smaller compared to the state-of-the-art implementations based on the first generation of polymorphic gates. Bi-functional image filters based on the newly designed gate sets were 30 – 39% smaller than implementations based on the first generation of polymorphic gates and also 19 – 34% smaller than implementations designed by conventional gates and conventional design approaches. In general, it was shown that it is possible to circumvent issues related to the gate-level synthesis of multifunctional circuits in applications involving design at the RT level by moving the synthesis one level up – from the gate level to the RT level. Furthermore, new efficient bi-functional circuits (new in the field of polymorphic electronics) were designed: increment/decrement, adder/subtractor.

Results in this thesis show that polymorphic electronics should be the concept which improves area-efficiency (price) of implementation of circuits with a second function not only at the academical level, but also in practice.

4.2 Developed library available online

As a part of the research, author of this thesis developed the *PoLibSi* library, which is available online at `www.fit.vutbr.cz/~inevoral/polibsi`. It is the first freely available library

with polymorphic gates ever. PoLibSi contains 38117 bi-functional gates with promising parameters, whose function is selected by the polarity of dedicated power rails. Individual gates are classified into the gate sets. The gate sets differ in the transistor type (MOSFET, double-gate ambipolar transistors), feature which the gate sets were optimised to (transistor count, delay, power consumption) and input impedance constraint. Each gate implementation comprises a schematic, an HSPICE description and simulation results. Moreover, the propagation delay and power consumption are provided for all MOSFET based gates. Figure 4.1 shows an example of gate details in the PoLibSi library. Furthermore, each gate set is complete – it provides at least one (usually even more) efficient implementation of any pair of two-input Boolean functions. The PoLibSi library can be later utilised for design and synthesis of complex bi-functional circuits by other researchers.

PoLibSi MOS_OPT_HI $\overline{a + b}/\overline{a \oplus b}$ (#k412)

Gate ID	Tr. count	Delay[1] [ps]	Power[2] [nW]
b1499	7	91	1174
b371	9	60	1030
g100	10	65	446
k412	11	26	434

Schematic

Note that if v_{dd} is connected to some parts of the gate, it is marked by 1V according to the simulations (see below).

HSPICE notation

```
*Xn source gate drain nMOS/pMOS
X1 vdd a J3 pMOS
X2 vdd b J0 pMOS
X3 vss b J0 nMOS
X4 vss a J3 nMOS
X5 pwr0 J0 J9 pMOS
X6 J3 J0 out nMOS
X7 J3 b out pMOS
X8 out J3 J0 nMOS
X9 pwr0 b J9 nMOS
X10 out a J9 nMOS
X11 J9 J3 out pMOS
```

HSPICE simulation

For HSPICE simulations of the gate, 45nm BSIM4 transistor models V1.0 from [1]

Figure 4.1: Screenshot of the PoLibSi library with details about NOR/XNOR gate with identifier k412 from the MOS_OPT_HI gate set.

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4.3 Future work

Besides the five attached papers, which form the core of the dissertation, power consumption of MOSFET-based gates from PoLibSi was already investigated together with different technology nodes (32nm, 45nm and 65nm) of MOSFET transistors. Furthermore, complex RTL components and several applications were designed and compared to both implementations with conventional gates only and implementations with polymorphic gates of the first generation. The results, summarised in Chapter 3.4 of this thesis, are currently submitted as one conference paper and one journal paper.

There are still some different ways how to further develop the research results:

- As soon as accurate models of double-gate ambipolar transistor will be freely available, the propagation delay and power consumption of designed gates can be determined in order to select the best implementation(s) of each polymorphic function.

- The PoLibSi library can be further extended by new gate sets based on other modern on emerging transistor types, e.g. FD-SOI, FinFETs or mono-gate (three-terminal) ambipolar transistors.

- The most promising method for synthesis of polymorphic circuits optimises the circuits in so-called PAIG data structure [13]. The method cannot perform technology mapping. It would be useful to develop a method which efficiently maps such circuits to two-input polymorphic gates with any functions, i.e. to the gates from the PoLibSi library. Such method may also take into account optimisation criteria as size, delay or power consumption.

- The PoLibSi library can be further extended by selected three- or more-input gates (e.g. AND3/OR3, NAND3/XNOR3, etc.) which may also be useful during the circuit synthesis.

- For further research related to the designed MOSFET-based gates and to the gates controlled by power supply polarity, a subset of PoLibSi gates can be designed at the layout level and employed in some integrated circuit similar to REPOMO32 [52] to definitely prove the concept on silicon.

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Related papers

Paper I

Evolutionary Design of Polymorphic Gates Using Ambipolar Transistors

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Evolutionary Design of Polymorphic Gates Using Ambipolar Transistors

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Abstract—**The objective of the paper is to introduce a new approach to the evolutionary design of polymorphic digital circuits conducted directly at transistor level. A discrete event-driven simulator was utilized to achieve reasonable trade-off between performance and precision. The proposed approach was evaluated on a set of polymorphic logic circuits controlled by switching the power rails. It was demonstrated that the proposed method is able to produce valid solutions. A lot of polymorphic gates based on ambipolar transistors were designed, which provide transistor savings compared to existing circuits. A new class of polymorphic gates was discovered thanks to the proposed system – gates based on conventional MOS transistors whose functions are changed by switching the power rails. They seem to have the best parameters among currently known polymorphic gates based on conventional transistors.**

I. INTRODUCTION

In some situations it would be useful to have one more logic function implemented in a digital circuit that is not needed during normal operation of the circuit, but could be activated occasionally under special circumstances. For example, it could be a test, a watermark, an emergency function or simply any hidden secondary required function. A conventional solution is to attach an additional circuit to the main circuit and simply activate it (or switch the output) when necessary. Another approach that usually brings more efficient and smart solution could be so-called polymorphic or multifunctional electronics.

Polymorphic electronics as an approach to design and implementation of multifunctional digital circuits was proposed by the team of A. Stoica at the NASA JPL about 15 years ago [1]. The main idea behind the Polymorphic electronics is to have a single structure (circuit) that is able to perform more than one logic function. The function just performed by the circuit (only one function should be performed by the circuit of course) depends on the circumstances of the circuit, on the state of the environment. Polymorphic circuits are created from polymorphic logic gates; the change of the whole circuit function is caused by the change of Boolean functions performed by used polymorphic gates. Interconnection of the circuit components (gates) remains unchanged. Therefore, polymorphism does not mean reconfiguration, components just change their behavior [2].

Utilization of the polymorphic electronics concept is limited by the existence of effective implementation of polymorphic gates. Typical environment which affects the function of a polymorphic gate is power supply voltage. The power supply rail cannot be only a means of energy distribution but also another channel for a global information distribution. The main advantage of such a function driver is that all gates already have the power supply voltage connected – no special wiring for a "change function" signal is needed.

In the past, the change of the function was driven by the level of supply voltage. For example, if the V_{dd} line was 3.3V above the ground, all polymorphic gates employed in the circuit perform one certain function. When the V_{dd} was 5V above the ground, polymorphic gates began to perform another function [3]. As these gates were often implemented using conventional CMOS technology, which is elaborated to provide stable behavior of logic gates, results were not always as effective as desired. In fact, these gates were designed as analog circuits with all disadvantages like high power consumption, slow operation etc.

In recent years, the research on polymorphic gates was focused on the utilization of so called post-silicon devices [4]. It seems that some features of post-silicon devices like ambipolarity may play an important role in the field of polymorphic electronics [5]. It enables to implement polymorphic gates using ambipolar devices – devices that are also naturally able to change their behavior. By this, the principle of polymorphism (as intended by Stoica [1] and their followers [3]) would now be moved one step towards more effective implementation of polymorphic circuits. Utilization of ambipolar devices as basic building blocks of polymorphic gates requires another way of power supply driving than the one proposed by Stoica et al. To change the polarity of ambipolar transistors, the polarity of the power supply must be reversed. This way of polymorphic gate function change leads to very efficient and neat implementation of logic gates, very close to the purity of ordinary CMOS logic gates. Parameters of such designed gates are also very promising, as the design is wholly digital – transistors operate as switches in the saturation mode.

Although the power supply rails switching as the way of polymorphism function driving was developed primarily for the gates based on ambipolar transistors, some gates using

only ordinary silicon MOS transistors were also developed and they also seem to be promising.

As it is already obvious from the text above, the design of polymorphic gates (and polymorphic circuits in general) is not a trivial task for a human designer especially due to the fact that more than one function must be kept in mind while the structure of the gate is proposed. Especially due to this fact, most of existing polymorphic gates are results of evolutionary based design [6], [7]. At the time of writing this paper no article describing evolutionary design of polymorphic gates based on ambipolar transistors was published.

In this paper, the evolutionary design of novel polymorphic gates is described and some promising results are shown. The paper is organized as follows: Section II introduces the field of polymorphic electronics and the problematics of polymorphic gates. In Section III, ambipolar transistors as basic blocks of some newly created polymorphic gates are briefly described. Section IV shows how polymorphic gates were evolved using CGP and Section V presents the results of evolution – newly created gates. Section VI concludes the paper.

II. POLYMORPHIC ELECTRONICS

The key to the circuit multifunctionality lies in the components, because these are the devices that change their function. Moreover, the change of the function exhibited by the component may be done by various ways. It may be advantageous if each component has its own sense to a phenomenon, which causes function change and the phenomenon is inherently present in the circuit (like supply voltage level, temperature etc.), then no special signal (distributed by a global interconnection network) is needed to control the function and the implementation of multifunctionality could be very natural.

The set of components typically consists of logic gates, so the structure of a polymorphic circuit is studied on the gate level of abstraction. Just gates make the difference between conventional logic and polymorphic circuits. The main two problems of the polymorphic electronics are:

- The problem of design methods (synthesis) for polymorphic circuits, i.e. how to map a description in the behavioral domain to a description in the structural domain. A lot of polymorphic circuits were designed using evolutionary design methods, especially using Cartesian Genetic Programming [6]. However, the non-evolutionary (conventional) design methods were also proposed [8].
- Search for suitable polymorphic components (gates). Implementation of the gate should be efficient (in terms of occupied chip area or transistor count).

Whereas the first problem is addressed by several papers in recent years and new synthesis methods arose, new gates for polymorphic electronics were published rarely in last years. The reason is perhaps the fact that conventional MOS transistors are very stable devices. Therefore, a trial to develop a multifunctional gate using silicon MOS transistors leads to a complicated structure with inferior parameters. Fortunately, new ambipolar devices promise development of new efficient

TABLE I
A SURVEY OF EXISTING SILICON-BASED CMOS POLYMPORPHIC GATES.

Gate	Control	Ctrld. by	Size	Ref.
NAND/NOR	3.3/1.8 V	V_{dd}	6	[2]
AND/OR	1.2/3.3 V	V_{dd}	8	[7]
NAND/NOR	5/3.3 V	V_{dd}	8	[3]
AND/OR	27/125 °C	temperature	6	[1]
AND/OR	5/90 °C	temperature	8	[1]
NAND/NOR	0/5 V	ext. voltage	10	[9]
NAND/NOR	5/0 V	ext. voltage	8	[10]
NAND/NOR	5/0 V	ext. voltage	10	[10]
NAND/XOR	5/0 V	ext. voltage	9	[10]
AND/OR	0/3.3 V	ext. voltage	6	[1]
AND/OR/XOR	3.3/1.5/0 V	ext. voltage	9	[1]
NAND/NOR	0/5 V	ext. voltage	10	[6]

and graceful gates with potentially very good electrical parameters and the research of them enables also a development of new gates based on ordinary silicon MOS transistors. So this paper contributes to the research just in the second of the two problems mentioned above.

A polymorphic gate is an element which realizes an elementary Boolean function, whereas the function may vary (for the same element) in accordance with the particular state of the environment. It is possible to say that the function of the gate is controlled by the environment. Such feature may be useful for variety of applications and may save the chip area and significantly reduce the global interconnections.

If the gate exhibits e.g. NAND function for some range of the power supply voltage (V_{dd}) and e.g. NOR function for another range of the V_{dd}, the gate could be specified as a NAND/NOR gate controlled by V_{dd}. It is assumed that polymorphic gate may perform no more than one function with respect to any particular instant during the course of time. Due to the fact that gate has just one output port available, it may deliver only single value from all the possible options at a time.

Table I surveys the polymorphic gates reported in literature. For each polymorphic gate, the logic functions performed by the gate are given together with recommended setting of the control signal variable. The number of transistors characterizes the size of polymorphic gates only partially (transistors occupy different areas, gates were fabricated using different fabrication technology).

Only two of the polymorphic gates have been fabricated so far; remaining polymorphic gates were either simulated or tested in a field programmable transistor array (FPTA-2). For instance, the 6-transistor NAND/NOR gate controlled by V_{dd} was fabricated in a 0.5-micron HP technology [2]. Another NAND/NOR gate controlled by V_{dd} and introduced in [3] was utilized in the REPOMO32 chip.

III. AMBIPOLAR TRANSISTORS

In the literature it was reported that many post-silicon devices developed in recent years exhibit so called ambipolar

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behavior. The principle behind the ambipolar behavior of a transistor is that the transistor operates like P-type conventional MOS transistor under certain conditions, but for example a corresponding adjustment of gate bias triggers its transition into N-type mode – it changes the behavior and operates like N-type conventional MOS transistor. This behavior seems to be very advantageous for complementary (CMOS like) structures and the fabrication of such structures may be very simplified – just one type of the transistor is used everywhere. The polarity of transistors in the structure (if the transistor is of P- or N-type) is then determined by the gate bias or by a special electrode [11].
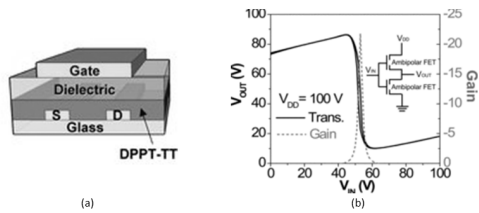
Fig. 1. (a) Stucture of ambipolar transistor from [12], (b) typical step response and gain of ambipolar inverter formed by two identical transistors.

Figure 1 shows a scheme of an ambipolar transistor, which is formed from diketopyrrolopyrroles-Thieno[3,2-b]thiophene copolymer [12]. But what is more important from the utilization in polymorphic structures is the typical step response and a gain of ambipolar inverter formed by two such transistors, also shown in Figure 1. Thanks to ambipolarity one transistor acts as a P-type transistor and the second one as an N-type, although they are both manufactured as identical devices.

The fact that the polarity of the ambipolar transistor is not determined by the fabrication process, but it could be changed by the gate bias (position of the transistor in the circuit towards supply voltage poles) or by a special electrode, should be used in development of polymorphic gates. Note that the inverter depicted in Figure 1 may exhibit the same behavior for both possible polarities of the power supply. This is because the inverter is symmetric and both transistors are the same. For non-symmetric and more complex gate structures (e.g. those aptly developed by an evolutionary algorithm) the behavior should be apparently more interesting.
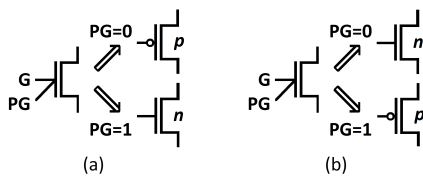
Fig. 2. Behavior of ambipolar transistor (a) type 1, (b) type 2.

The evolutionary design described in this document is based on ambipolar transistors with special electrode known as polarity gate (PG). These transistors have been reported in several emerging technologies such as carbon nanotubes (CNTs), graphene and silicon nanowires (SiNWs) [13].

The behavior of ambipolar transistors vary according to the used technologies [13], [14]. It can be divided into two different categories:

- **Type 1:** These transistors act as N-type in case of logic 1 at PG pin and P-type in case of logic 0 – Figure 2a).
- **Type 2:** These transistors act as P-type in case of logic 1 at PG pin and N-type in case of logic 0 – Figure 2b).

IV. EVOLUTIONARY DESIGN OF GATES

Several polymorphic gates using ambipolar transistors were already designed [15], but no systematic design methods were ever described. Moreover, only few papers were devoted to evolution of small digital circuits directly at transistor level in general utilizing standard p-MOS and n-MOS devices.

Zaloudek et al. published an approach based on a simple simulator which was designed to quickly evaluate the candidate solutions [6]. Unfortunately, a rough approximation of transistor behavior caused that this approach produced many incorrectly working circuits. Trefzer used another technique to evolve some basic logic gates [16]. Instead of using a time consuming analog circuit simulator, a reconfigurable analog transistor array was employed. However, it was shown that many of the discovered solutions relied on some properties of the utilized reconfigurable array. About 50% of the evolved circuits failed in the analog simulation. Walker et al. used a different technique to evolve transistor-level circuits [17]. In order to speed up the time consuming evaluation of candidate solutions, a cluster of SPICE-based simulators was utilized. Even if it was possible to evolve correct solutions, only small problem instances could be investigated due to the overhead of SPICE simulators. In order to obtain circuit working in the analog simulation in reasonable time, Mrazek and Vasicek proposed a discrete simulator with a switch-level transistor model extended by a threshold drop degradation effect to achieve a fast simulation with reasonable accuracy [18]. In this paper, such evolutionary method was proposed. The proposed approach reflects a different functionality of the ambipolar transistors and utilizes a new circuit representation and simulation.

A. Circuit representation

In order to evolve polymorphic circuits at the transistor level a suitable representation enabling to encode bidirectional graph structures containing junctions is needed. We utilized a Cartesian genetic programming (CGP) proposed by J. Miller [19].

The proposed representation proceeds from CGP representation of gate-level circuit. It is defined as follows. Each polymorphic digital circuit having n_i primary inputs and n_o primary outputs (i.e. a candidate solution) is represented using an array of nodes arranged in n_c columns and n_r rows. Each node consists of three source terminals and one output terminal. Each node can act as p-MOS transistor, n-MOS transistor, ambipolar transistor or a junction. Ambipolar transistor uses all three source terminals, whereas the rest of nodes two source terminals only. The utilized nodes are

shown in Figure 3. Source terminals of each node can be independently connected to the output terminal of any node placed in previous l_{back} columns. In addition to that, source terminals of each node can be connected to one of the primary circuit inputs.
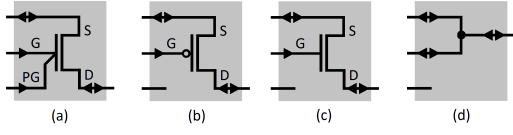

Fig. 3. Basic building blocks of transistor-level circuits: (a) ambipolar transistor, (b) p-MOS transistor, (c) n-MOS transistor and (d) junction that combines three signals together. If a proper voltage is applied on the gate electrodes denoted as G and PG, transistor connects its source electrode (S) with drain (D). The arrows denote the possible directions of signal flow which have to be considered during the evaluation.

The junction nodes combine two input signals and one output signal together. As a consequence of that, loops and multiple connections are natively supported.

The following integer encoding scheme so-called chromosome is utilized. The primary inputs are labeled from 0 to $n_i -1$ and the node outputs from n_i to $n_i + n_c \cdot n_r - 1$. A candidate solution is represented in the chromosome by $n_c \cdot n_r$ quaternion (x_1, x_2, x_3, f) determining for each node its function $f \in \Gamma$, where $\Gamma = \{0^{ambipolar}, 1^{p-mos}, 2^{n-mos}, 3^{junction}\}$ is a function encoding, and label of nodes x_1, x_2 and x_3 connected to the input terminals. The last part of the chromosome contains n_o labels of nodes where the n_o primary outputs are connected to. Note that the power supply rails are explicitly encoded as the first two primary inputs.

Figure 4 demonstrates the principle of utilized encoding on a polymorphic inverter circuit which inverts the logical value of input signal independently of power rails switching. The shown chromosome encodes a candidate circuit using four nodes. However, only three of them contribute to the phenotype and are active.
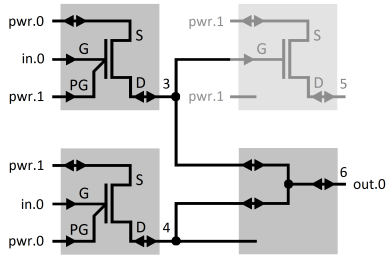
Fig. 4. Example of an encoding of a candidate circuit implementing polymorphic inverter using two ambipolar transistors. Parameters are as follows: $n_i = 3$ *(pwr.0, pwr.1, in.0)*, $n_o = 1$ *(out.0)*, $n_c = n_r = l_{back} = 2$. The integer chromosome is *(0,2,1,0)(1,2,0,0)(1,3,1,2)(3,4,4,3)(6)*.

B. Transistor discrete model

As stated in Section III, the research of ambipolar transistors started a few years ago. As a consequence of that, no exact models are still available. Therefore, we created two discrete models of ambipolar transistor according to the expected behavior.

The first model of ambipolar transistor utilizes standard MOS transistor behavior extended to a special PG pin which switches the transistor polarity. The transistor behavior corresponds to the TSMC technology $\lambda = 0.25$ μm used by Mrazek and Vasicek [18]. The MOS model is based on the switch-level transistor model extended to a threshold drop degradation effect, it is abstracted from dynamic parameters such as power consumption or delay. The simulation uses six voltage levels: logic 0 (denoted as '0'), logic 1 ('1'), degraded 0 ('L'), degraded 1 ('H'), high impedance ('Z') and undefined value ('X'). The behavior of n-MOS and p-MOS transistors is defined by Table II, which determines the drain level value from level values of gate and source. The ambipolarity of the transistor is obtained by the state of the PG pin. We defined two types of the model: type 1 is defined as follows: (a) If value at PG pin is '1' or 'H', transistor acts as n-MOS, (b) if value at PG pin is '0' or 'L', transistor acts as p-MOS (c) otherwise drain level voltage is 'X'. Similarly, the behavior of ambipolar transistor type 2 is defined as follows: (a) If value at PG pin is '1' or 'H', transistor acts as p-MOS, (b) if value at PG pin is '0' or 'L', transistor acts as n-MOS (c) otherwise drain level voltage is 'X'. In this paper, polymorphic circuits evolved using this model are called as circuits with six-state logic.

TABLE II
BEHAVIOR OF N-MOS AND P-MOS TRANSISTORS MODELED USING SIX DISCRETE VALUES.

	n-MOS							p-MOS					
gate	source						gate	source					
	1	H	L	0	Z	X		1	H	L	0	Z	X
1	H	X	L	0	Z	X	1	Z	Z	Z	Z	Z	X
H	X	X	L	0	Z	X	H	Z	Z	Z	Z	Z	X
L	Z	Z	Z	Z	Z	X	L	1	H	X	X	Z	X
0	Z	Z	Z	Z	Z	X	0	1	H	X	L	Z	X
Z	Z	Z	Z	Z	Z	X	Z	Z	Z	Z	Z	Z	X
X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table III defines the n-MOS and p-MOS transistors behavior of the second model. This model is stricter than the first one – the transistor does not have to recognize the degraded value at G and PG pins well. The degraded values are not propagated from source to drain. The behavior of ambipolar transistor type 1 is defines as follows: (a) If value at PG pin is '1', transistor acts as n-MOS, (b) if value at PG pin is '0', transistor acts as p-MOS (c) otherwise drain level voltage is 'X'. Similarly, the behavior of ambipolar transistor type 2 is defined as follows: (a) If value at PG pin is '1', transistor acts as p-MOS, (b) if value at PG pin is '0', transistor acts as n-MOS (c) otherwise drain level voltage is 'X'.

The second model utilizing six logic values can be optimized to four-state logic as follows. When the value at both G and S pins is '1', the value of n-MOS drain is 'H' (similarly, '0' at both gate and source terminals of p-MOS produces 'L' at drain). These degraded values cannot be used in the evolved

TABLE III
BEHAVIOR OF N-MOS AND P-MOS TRANSISTORS MODELED USING SIX
DISCRETE VALUES. THIS BEHAVIOR IS USED TO GET FOUR-STATE LOGIC.

	n-MOS						p-MOS					
	source							source					
gate	1	H	L	0	Z	X	gate	1	H	L	0	Z	X
1	H	X	X	0	Z	X	1	Z	Z	Z	Z	Z	X
H	X	X	X	X	Z	X	H	X	X	X	X	Z	X
L	X	X	X	X	Z	X	L	X	X	X	X	Z	X
0	Z	Z	Z	Z	Z	X	0	1	X	X	L	Z	X
Z	Z	Z	Z	Z	Z	X	Z	Z	Z	Z	Z	Z	X
X	X	X	X	X	X	X	X	X	X	X	X	X	X

circuit, because the transistors do not accept these values and a degraded value at circuit primary output is also undesirable. The only one possibility of occurrence is a junction of the degraded and non-degraded value. As a consequence, more circuits can be evolved by this model than by a pure four-state model. Because the transistors are not controlled by degraded values, polymorphic circuits evolved using this model are called as circuits with four-state logic in this paper.

C. Evaluation of the candidate solutions

The goal of the evaluation is to determine that the candidate circuit meets the requirements i.e. there is no constraint violated and the circuit works correctly w.r.t. definition. Evaluation of the candidate solutions encoded using the proposed representation consists of two steps.

Firstly, set of active nodes is determined. This operation is performed due to speed optimization and because of skipping of exceptions like short circuits in the unused part of the circuit. Only the active nodes represent (i.e. they are in a path from input nodes to outputs) the evaluated circuit. Inactive nodes are ignored. A node is active if either (a) its output is connected to any of the primary outputs, or (b) its output is connected to an active node, or (c) it is a junction node whose at least one source terminal is connected to an active node.

Then, multi-level discrete event-driven simulator is utilized to determine the response for each input combination. The advantage of this approach is that only necessary nodes are updated if there is a change of a value.

The following steps are used to determine output value for a given input combination. Firstly, outputs of all nodes are initialized to the value 'Z'. Then, values 0 and 1 (according to the currently simulated input combination) are assigned to the primary inputs. This change triggers re-evaluation of all the nodes connected directly to primary inputs. Each node determines its new output value and propagates it to all related nodes. As an open transistor connect source with drain, bidirectional data-flow have to be utilized. It means that the new value must be propagated to the nodes connected not only to the drain but also to source terminal. Similarly, junctions have to propagate the new value to all terminals. The new value of a junction node is calculated as the strongest value presented on all the terminals. The new value of a transistor node is determined according to the value connected to the source as

well as drain. During the evaluation of a new output value of a transistor node, the new calculated value is compared with current value at drain terminal. If the values are not compatible, short circuit exception is raised. Otherwise, the stronger value is propagated to all related nodes. The relations between the discrete values are as follows: 'Z' $\prec$ 'L' $\prec$ '0' $\prec$ 'X'; 'Z' $\prec$ 'H' $\prec$ '1' $\prec$ 'X'. It means that if at least one of the values is equal to 'X', 'X' is propagated to all related nodes.

D. Search strategy

The overall CGP design algorithm is shown in Algorithm 1. As a search algorithm, $1 + \lambda$ evolutionary strategy is utilized [19]. The initial population is randomly generated. Every new population consists of the best individual and λ offspring created using a point mutation operator which modifies h randomly selected genes. When two or more best individuals of the population receive the same fitness as the highest score of the previous population, one of the best individuals which did not serve as a parent in the previous population is randomly selected as a new parent. This strategy is used to ensure the diversity of population. The evolution is terminated when a predefined number of generations is reached.

Algorithm 1: CGP design

Input: CGP parameters, fitness function
Output: The highest scored individual p and its fitness

1 $P \leftarrow$ randomly generated p and its λ offspring;
2 EvaluatePopulation(P);
3 **while** ⟨*terminating condition not satisfied*⟩ **do**
4      $\alpha \leftarrow$ highest-scored-individual(P);
5   **if** *fitness(α) $\geq$ fitness(p)* **then**
6          $p \leftarrow \alpha$;
7      $P \leftarrow$ create λ offspring of p using mutation;
8   EvaluatePopulation(P);
9 **return** p, fitness(p);

Quality of each candidate solution is determined by the *fitness function*. For evolution of polymorphic circuits, all possible input combinations have to be applied at the candidate circuit inputs. The obtained output values are compared with corresponding required truth table and the goal is to minimize the Hamming weight. The fitness value is constructed as follows: If an obtained output value corresponds to the expected one, 5 points are added to the fitness value. If the calculated value exhibits the same polarity but represents degraded voltage, 2 points are used. Otherwise, no point is added because the response is invalid. If there is a short-circuit exception during the simulation, the simulation is terminated and 3 points penalty is subtracted from the total fitness value. Similarly, if the simulator exceeds the predefined number of steps (i.e. node outputs are not in stable state), the simulation is terminated and the fitness value is penalized by 3 points.

Evolved circuits can connect the primary input signals through the transistors directly to the primary outputs. Such

circuits does not provide high input impedance and low output impedance, which is required. In order to avoid this fact, we defined two types of constraints for evolved circuits:

- *High-Impedance (HI)* - Primary signal inputs can be routed to source and drain transistor terminals, but no input combination can cause connecting of any primary input signal to primary output of the evolved circuit. This constraint is for *high input-impedance and low output-impedance*.
- *Extra High-Impedance (Extra-HI)* - Primary signal inputs can be routed to gates and polarity gates of transistors only. This constraint is used for the same impedance requirements, but it is stricter than previous one.

As soon as a fully working solution is found, additional requirements (like e.g. high input impedance and low output impedance) for circuit properties can be checked. Only a fully working candidate circuit with desired properties may replace the current best individual.

As soon as a fully working solution with desired properties is found, i.e. it meets the specification, optimization of circuit size starts. Only a fully working candidate circuit with desired properties and equal or less utilized transistor may replace the current best individual.

V. EVOLVED GATES

The proposed method was evaluated in the evolution of basic polymorphic logic circuits controlled by switching the power rails. The goal of the experiments was to evolve fully functional implementations of 36 polymorphic circuits exhibiting full voltage swing on the outputs. These circuits were evolved with different transistor types – (a) MOSFET transistors only, (b) ambipolar transistors only and (c) MOSFET and ambipolar transistors. In addition to that, the impact of High-Impedance and Extra High-Impedance constraints were investigated. Finally, the ability of evolutionary algorithm to find the solution is demonstrated.

The results were obtained from more than 300 independent runs for each combination of polymorphic gates, used types of transistors and additional constraints using the following experimental setup: CGP matrix size: 5x5, $l_{back} = 5$, mutation: $3 \simeq 4\%$, number of generations: 2,000,000.

A. Polymorphic gates with MOSFET and ambipolar transistors

Firstly, it was necessary to find out, which polymorphic gates we are able to evolve with six-state logic transistor model without any constraints. We chose all 36 polymorphic gates created as a product of identity (denoted as ID), negation (NOT) and basic two input gates (AND, NAND, OR, NOR, XOR, XNOR). Note that ID/ID gate marks polymorphic multiplexer and NOT/NOT marks polymorphic inverter. As you can see count of transistors in Table IV, all evolved polymorphic gates using six-state logic and both MOSFET and ambipolar transistors type 1 were found. Moreover, the most difficult OR/OR gate needs 9 transistors only.

TABLE IV
SIZE OF THE SMALLEST FOUND SOLUTION OF POLYMORPHIC GATES
f_1/f_2 UTILIZING MOSFET AND AMBIPOLAR TRANSISTORS TYPE 1

f_1	f_2							
	ID	NOT	AND	NAND	OR	NOR	XOR	XNOR
ID	4	4	7	6	7	6	8	8
NOT		2	6	6	6	6	7	7
AND			5	7	5	7	7	7
NAND				4	7	4	7	7
OR					9	7	7	7
NOR						4	7	7
XOR							6	4
XNOR								6

When the circuits are designed, it is appropriate to use the same types of transistors and not to combine different technologies, because the combination of technologies complicates the manufacture of the circuit.

B. Polymorphic gates with MOSFET transistors only

As it was written in Section II, several polymorphic gates using MOSFET transistors were already published. These gates were analog designs with all failings like high power consumption, slow operation etc. However, digital approach to polymorphic circuits based on MOSFET have not ever been presented.

Table V shows that a lot of such polymorphic gates based on TSMC 0.25 μm transistors can be created. We can see that it is more difficult to find polymorphic gates using MOSFET transistors only, because the found solution utilize more transistors. Moreover AND/OR and NAND/NOR gates were not found in any of 300 runs.

TABLE V
SIZE OF THE SMALLEST FOUND SOLUTION OF POLYMORPHIC GATES
f_1/f_2 UTILIZING MOSFET TRANSISTOR ONLY

f_1	f_2							
	ID	NOT	AND	NAND	OR	NOR	XOR	XNOR
ID	4	4	7	7	7	7	8	8
NOT		6	6	8	6	8	10	10
AND			9	8	-	9	12	10
NAND				8	9	-	10	12
OR					9	8	10	11
NOR						8	11	10
XOR							9	12
XNOR								9

C. Polymorphic gates with ambipolar transistors only

Many digital circuits based on ambipolar transistors have already been published [14]. However, only few polymorphic circuits composed of these transistors were designed. Yang et al. presented NAND/NOR and XOR/XNOR gates [15]. Both gates use 4 transistors only. However, the second one expects the presence of both input signal negation. Therefore, 4 transistors and 2 inverters are needed (i.e. 8 ambipolar transistors in total). AND/OR gate have not ever been presented, but it can be simply assembled using 6 transistors from NAND/NOR gate and polymorphic inverter.

TABLE VI
SIZE OF THE SMALLEST SOLUTION OF SELECTED POLYMORPHIC GATES
UTILIZING AMBIPOLAR TRANSISTOR ONLY

Gate	Constraint	Type 1 6-state	Type 1 4-state	Type 2 6-state	Type 2 4-state
NOT/NOT	-	2	2	2	2
NOT/NOT	Extra-HI	2	2	2	2
NAND/NOR	-	4	4	4	4
NAND/NOR	Extra-HI	4	4	4	4
AND/OR	-	5	5	3	3
AND/OR	Extra-HI	6	6	4	4
XOR/XNOR	-	4	5	5	5
XOR/XNOR	Extra-HI	6	8	5	6

We also tried to evolve polymorphic circuits based on ambipolar transistors only. Four polymorphic gates from 36 mentioned above were successfully evolved: NAND/NOR, AND/OR, XOR/XNOR and polymorphic inverter. Table VI shows the minimal transistor count needed for design of these gates. As you can see, Extra-HI constraint causes increase of utilized transistors. Similarly, 4-state logic uses equal or more resources.
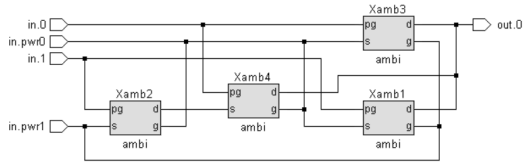
Fig. 5. AND/OR polymorphic gate with Extra-HI restriction based on ambipolar transistors type 2.

All the evolved gates need equal or less ambipolar transistors in comparison with gates mentioned above. Evolved inverter and NAND/NOR gate do not provide any transistor savings compared to the known solutions. However, various combinations of transistor models and impedance constraints provide polymorphic gates with significantly lower number of ambipolar transistors. Four transistors are needed to design the XOR/XNOR gate and even just three transistors are needed to design the AND/OR polymorphic gate.
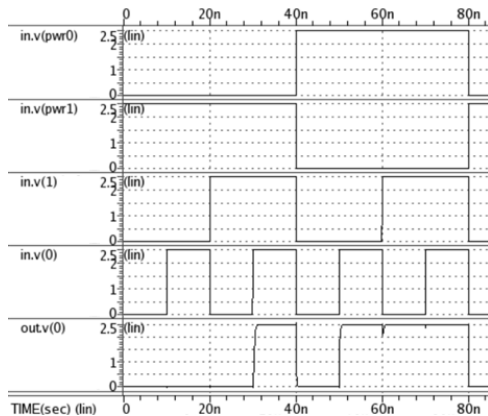
Fig. 6. HSPICE simulation result of polymorhic and/or gate from Figure 5.

As an example, Figure 5 shows the AND/OR polymorphic circuit with Extra-HI constraint controlled by switching the power rails. It is composed of four ambipolar transistor type 2.

All discovered circuits were verified using a HSPICE simulator. Nowadays, HSPICE model for ambipolar transistor with special electrode is not available. Ambipolar behavior was emulated by a circuit composed of two MOSFET transistors, two transmission gates and one inverter. All the circuits were valid and operated correctly. Figure 6 shows the HSPICE simulation results of the AND/OR gate from Figure 5.

D. Space-Search method results

The aim of the paper is to prove that modified CGP is able to design a new polymorphic circuits utilizing models of ambipolar transistors. In previous sections, we have shown that the proposed method have found working solutions for various types of transistors.

Figure 7 describes the following parameters during the evolution of all 300 independent runs of design. First parameter is size of fully functional solutions. We observe minimal, maximal and average count of transistors. We also observe the success rate, which represents how many runs have found fully functional circuit that meet the specified constraint in current generation.

We can see that Extra-HI constraint reduces the performance of the evolution. Substantially higher number of generations is needed to achieve the same success rate. Moreover, when a new working solution is found, the size quickly decreases to the minimal one (see the width of size-peeks). In addition to that XOR/XNOR gate is a more difficult problem to solve than AND/OR.

Interestingly, when we compare unconstrained runs and different types of models, the 4-state logic provides worse success rate shape than the 6-state logic. Moreover, ambipolar transistor type 2 provides better success rate than type 1 – approx. twice more generations are needed to obtain the same success rate. However, all configurations tend towards the same results, but the speed is different.

VI. CONCLUSION

A new approach suitable to the evolutionary design of polymorphic digital circuits conducted directly at transistor level was introduced in this paper. In order to improve the time consuming evaluation of candidate solutions, a discrete event-driven simulator was utilized. The proposed simulator operates on multiple logic levels to achieve reasonable trade-off between performance and precision. Two discrete voltage level models of polymorphic logic were presented, which have a potential to be used in many other simulations of polymorphic circuits. The goal of the evolutionary algorithm is to design a circuit having the minimal number of transistors. In addition to that, various constraints on the evolved circuits are investigated to increase the success rate of the evolutionary design.

The proposed approach was evaluated in the evolution of polymorphic logic circuits controlled by switching the power
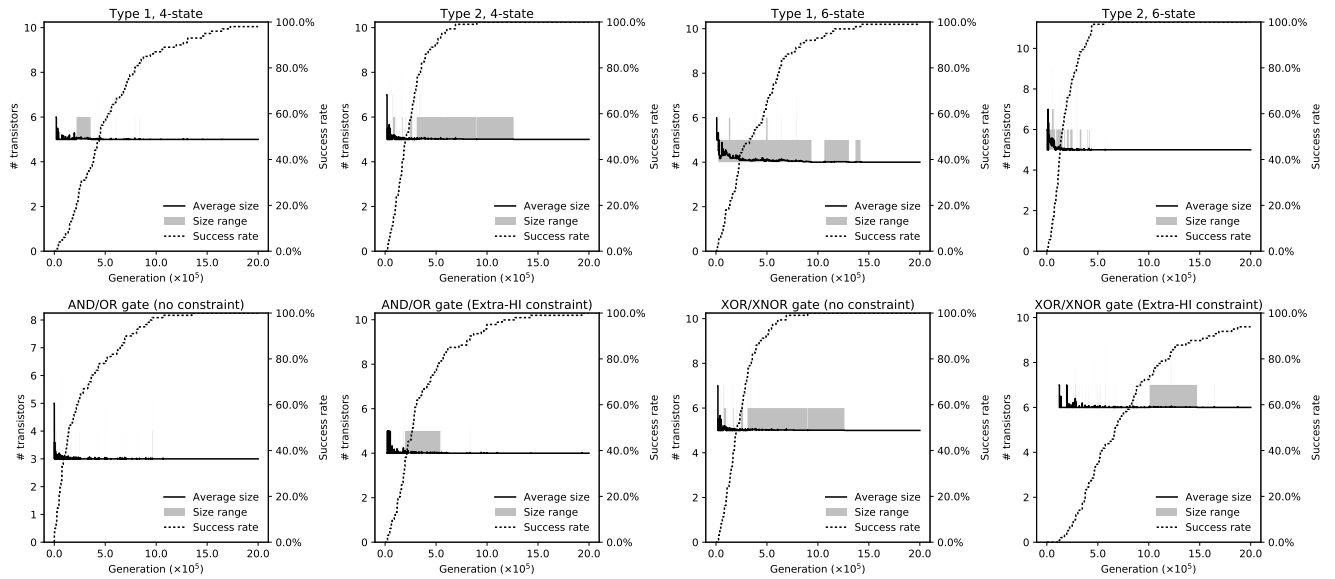
Fig. 7. Success rate and circuit size (minimal, maximal and average). First row shows values for various ambipolar models for XOR/XNOR unconstrained runs. The second row shows results for impedance constraints used in evolution of AND/OR and XOR/XNOR ambipolar circuits utilizing 4-value logic type 2 ambipolar transistors.

rails. It was demonstrated that the proposed method is able to produce valid solutions. A lot of polymorphic gates controlled by switching the power rails and utilizing ambipolar transistors were designed, which provide transistor savings compared to existing circuits.

Thanks to the proposed system, a new class of polymorphic gates was discovered – gates based on conventional MOS transistors whose functions are changed by switching the power rails. They seem to have the best parameters among currently known polymorphic gates based on conventional transistors. This class of polymorphic gates may allow to use the polymorphic electronics also in existing chips (f. e. when additional PUF, watermark or hidden diagnostics is required) without any change of chip manufacturing technology.

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Paper II

CMOS Gates with Second Function

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CMOS Gates with Second Function

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Abstract—**In this paper, a new approach to design of multi-functional digital circuits is presented. It is based on adoption of polymorphic electronics paradigm which permits digital circuits to exhibit more than one function while preserving the same structure. In that case only components of the circuit (gates) have to be multifunctional. Individual gates have typically built-in sensitivity to the occurrence of some phenomena invoking the function change (e.g. power supply level etc.), which means that no dedicated net is required for that purpose. One of the key advantages of such circuits is the efficiency in terms of size. In this paper, MOS transistors are exploited in an unconventional manner where the circuit function selection depends just on the condition of power supply voltage rails, which is otherwise typical for polymorphic circuits utilizing ambipolar transistors. Furthermore, a first complete set of successfully simulated two-input polymorphic gates was obtained. These gates show the best parameters of all the previously published polymorphic gates – high input impedance and low output impedance, short time of signal propagation, low power consumption and low transistor count being used. Wide range of proposed polymorphic gates (function combinations) may help to obtain more efficient results during synthesis.**

Index Terms—**Polymorphic electronics, MOSFET, polymorphic gate, digital circuit, gate set.**

I. INTRODUCTION

Nowadays, significant majority of logic circuits are typically realised by means of using widespread CMOS technology. Although the first physical implementation of CMOS-based logic circuit has been successfully demonstrated more than 55 years ago [1] and a plenty of research activities have been carried out in the meantime, this technology still prevails as the major choice even in case of the cutting-edge electronic devices. In fact, last several decades have brought only a minor advancement regarding the structural and implementation aspects of basic Boolean functions (logic gates) in CMOS technology. When it comes to the target implementation size of logic circuitry, CMOS gates seem to be very optimal (only few transistors are needed to implement a Boolean function), thus, even very complex behaviour can be realised on a small silicon die. In order to accomplish higher functional density (more features within a similar chip area or amount of transistors), the reconfiguration scheme is sometimes used.

Another idea, how to increase functional density of a digital circuit, was proposed by the team of Adrian Stoica from NASA JPL [2]. This concept is called Polymorphic Electronics and its foundation is based on changing the function of circuit elements while their structure (and mutual interconnection) are preserved. This is in contrary to the principles of classic reconfiguration, where the change of circuit structure is the key for invoking another function. Ability of circuit function changing always incurs additional overhead. But in general, if the overhead is smaller than a cost of two (or more) circuits representing the intended functions, the resulting functional density is higher.

In case of classic reconfiguration, the associated overhead becomes evident in both space and time domain [3]. Polymorphic circuits typically have no time overhead (the function change is immediate) [4] and, moreover, overhead in the size domain is mostly smaller than for a classic reconfiguration. This is given by the fact that structure comprising a lot of switches or multiplexers is typically needed for reconfiguration purposes, as well as corresponding memory resources for storing the configurations. Neither additional memory nor dedicated reconfigurable structure pattern is needed for polymorphic electronics. If the synthesis of a polymorphic circuit is performed cleverly, the cost paid for an additional function could be very low [5].

Utilization of the polymorphic electronics concept as an approach how to design circuits with increased functional density, in comparison to conventional CMOS-oriented techniques, strongly depends on satisfying two principal conditions. First is given by the existence of suitable synthesis methods which are able to found one highly optimized structure for all intended functions. There have been recently proposed several approaches [6] – [7] how to surmount this obstacle.

Second condition is given by the availability of an efficient implementation of polymorphic gates, which should be able to change their functions in accordance to some well-defined and well-controllable global circumstances. However, the change of function for all gates in the circuit should require only minimal overhead when it comes to the propagation of such stimulus. Ideally, no dedicated global net is used for distributing the information about function change to the individual gates. It could be fulfilled for example by means of using power rail as a channel for function-change information distribution. In this case, polymorphic gates with the ability to change their function in accordance to the state of power supply voltage, should be employed [8]. Typically, polymorphic gates exhibit different functions for different levels of supply voltage.

One of the main problems connected with the practical

adoption of this approach is given by the analogue nature of the change itself. Such evidence subsequently leads to rather analogue design concepts projected into the polymorphic gates rather than staying in purely digital domain. The result is that some transistors work in a linear mode or short power supply. In this paper, another approach to the design of polymorphic gates controlled by the condition of power supply rail is proposed. This novel approach simply avoids the previously outlined pitfalls of analogue behaviour embedded into formerly proposed polymorphic gates because all transistors are either closed or in saturation and the nature of gates, as well as the indication of function change sent along the power supply rail, is handled in purely discrete way.

The paper is organized as follows: Section II introduces the field of polymorphic electronics and various aspects related to the design of polymorphic gates. New approach to multifunctional digital circuits is proposed in Section III together with a brief description of an evolutionary method used for design of new gates. In Section IV, set of designed polymorfic gates is presented. Finally, Section V provides a conclusion of this paper.

II. POLYMORPHIC ELECTRONICS

Polymorphic circuit represents specific type of a digital circuit that exhibits the natural ability to operate in two or more intentionally specified modes, when different (logic) function is performed in each of them. The structure (interconnections between individual components in such circuit) remains unchanged for all the permissible modes/functions. It is important to emphasize at this point that the multifunctionality itself is not achieved by means of exploiting the reconfiguration scheme for the actual circuit structure, but instead of that the change of behaviour (logic function performed) takes place for some components.

The swap of the function may be arranged in various ways. It could be advantageous (and somewhat typical scenario for polymorphic electronics) if each component demonstrates its sensitivity to a specific phenomenon responsible for the function change. It turns out to be very useful if such phenomenon is inherently present in the circuit (like supply voltage level, temperature etc.). Then, the circuit changes its function in accordance with those circumstances and no special signal (distributed by a global interconnection network) is needed to control this process. Such arrangement helps to keep the overhead paid for "extra" functions low.

The mechanism described above, responsible for the change of polymorphic circuit function, implies the existence of some application domains in which such kind of behaviour may help to get significant advantages. In general, these circuits could be used e.g. for:

- adaptation of the circuit behaviour to variable conditions with the target environment,
- reduction of power consumption or heat dissipation in order to preserve at least the essential circuit functionality, when energy goes low or temperature goes high,

- storing or hiding "extra" functions used as a watermark or other special features [2],
- embedded diagnostics purposes.

It is possible to recognize one important aspect shared across the various application areas of polymorphic electronics suggested above: There typically exists so called primary function, which needs to be implemented first, and another "additional" or "extra" function that might become desirable in some situations or under specific circumstances only. Although the concept of polymorphic electronics generally enables the possibility to have several equally important functions implemented in one circuit, just one main and one or more auxiliary, temporary, supplementary or emergency function are implemented due to practical reasons. In those cases, little bit more complicated or unusual manner of function change doesn't bring any major restrictions.

A. Polymorphic gates

Structure of a polymorphic circuit is typically studied on the gate level of abstraction. Just the gates themselves make the obvious difference between conventional logic and polymorphic circuits. Two main problems of the polymorphic electronics are:

1) The problem of design (synthesis) methods for polymorphic circuits, i.e. how to map a description in the behavioural domain to a description in the structural domain. A lot of polymorphic circuits were designed using evolutionary-based methods, especially those involving Cartesian Genetic Programming [9]. But also non-evolutionary (conventional) design methods were proposed [7].
2) Search for suitable polymorphic components (gates). Implementation of the gate should be efficient (in terms of occupied chip area or transistor count).

The emergence of new gates suitable for polymorphic electronics have been reported very rarely during last years. Most of them are based on unconventional devices or technologies like organic ambipolar transistors [10], nanoelectronic devices [11] etc. These devices allow to realise the changes in behaviour of the circuit at low levels within the design hierarchy – mostly at physical level.

The reason, why multifunctional or polymorphic gates based on CMOS were overlooked, lies in the fact that conventional MOS transistors, used as switches, are very stable devices. Thus, an attempt to develop a multifunctional gate using silicon MOS transistors mostly leads to a complicated structure with inferior parameters. On the contrary, new ambipolar devices hold a significant promise of developing new efficient and highly-refined gates with potentially very good electrical parameters [11]. The research of polymorphic gates utilising ambipolarity of transistors as the way how to switch between two function exhibited by the gate enables also development of new gates based on conventional silicon MOS transistors as described further in this paper.

Rich set of findings and observations gathered throughout numerous experiments with published polymorphic gates, as

well as with in-house design of several novel polymorphic gates and practical experiments with applications of digital polymorphic electronics, have allowed to formulate properties and criteria which should be fulfilled by polymorphic gate:

1) high input resistance (the gate must avoid the excessive overloading of previous logic net generated by its inputs),
2) low output resistance (the aim is to achieve unambiguously defined logic levels at the gate and let them closely follow, if possible, the potential of supply source irrespective of the actual output load caused by subsequent logic net, whereby maintaining reasonable circuit noise immunity),
3) short time of signal propagation – definition based on measurement of transfer path delay between input and output ports (t_{pd}),
4) low power consumption,
5) small dimensions.

III. APPROACH TO THE CIRCUIT DESIGN

Polymorphic gates, as proposed in this paper, are implemented by means of using conventional MOS transistors, when the circuit behaviour depends on the polarity of supply voltage. More accurately, the second circuit function is available when the electric potentials on the power supply rails are swapped.

In order to design new polymorphic gates, evolutionary approach proposed earlier in [12] was further refined and used in the context of this contribution. To achieve a fast simulation with reasonable accuracy, a discrete simulator with switch-level transistor model extended by a threshold drop degradation effect corresponding to $45nm$ technology is utilized. Moreover, this approach is capable of designing circuits with high input impedance and low output impedance. The resulting circuits are optimized with regard to the overall number of transistors being used.

Depending on the overall chip (or application circuit) design and usage of the second circuit function, whole circuit may consist of polymorphic gates only or it can exploit the combination of conventional and polymorphic parts. One of the key prerequisites for implementation of any Boolean function is the availability of a Boolean constant in the circuit. Normally, this requirement is fulfilled implicitly by the presence of power supply rails because their upper and lower threshold voltage levels equals to Boolean values. But in the situation when voltages on power supply rails could be swapped mutually, what is the constant?

Gates proposed in this paper need to have a Boolean constant connected somewhere inside the structure or on some input. For example, discrete switch-level transistor model used in the design approach assumes valid connection of transistor substrates – n-MOS to the negative power supply (gnd), p-MOS to the positive one. Therefore, although two supply wires are enough for the circuit in this type of polymorphic electronics, the voltage needs to be rectified internally. The actual way of rectification is usually application- and chip-specific. A generic solution can be accomplished by taking an advantage of the P-N transitions in the chip silicon, e.g. using one n-MOS and one p-MOS structure.

A. Circuit representation

In order to evolve polymorphic circuits at the transistor level a suitable representation enabling to encode bidirectional graph structures containing junctions is needed. We utilized a Cartesian genetic programming (CGP) proposed by J. Miller [9].

The circuit representation is derived from the CGP representation of gate-level circuit. Each polymorphic digital circuit is represented using an array of nodes and can be encoded by fixed length array of integers. Each node consists of two source terminals and one output terminal and can act as p-MOS transistor, n-MOS transistor or a junction. The utilized nodes are shown in Figure 1. Source terminals of each node can be independently connected to the output terminal of any node placed in previous columns or to one of the primary circuit inputs.
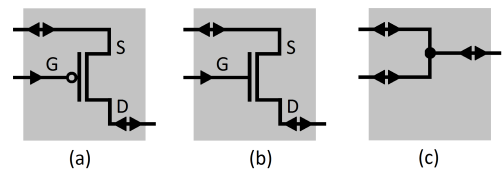

Fig. 1. CGP nodes of transistor-level circuits: (a) p-MOS transistor, (b) n-MOS transistor and (c) junction that combines three signals together. The arrows denote the possible directions of signal flow which have to be considered during the circuit evaluation.

The junction nodes combine two input signals and one output signal together. As a consequence of that, loops and multiple connections are natively supported.

Figure 2 demonstrates the principle of utilized encoding on a $in.0/1$ pass-logic polymorphic gate which provides identity of the only input signal as a first polymorphic function ($pwr.0 = gnd$, $pwr.1 = v_{dd}$) and a logic one as the other polymorphic function ($pwr.0 = v_{dd}$, $pwr.1 = gnd$). The shown chromosome encodes a candidate circuit using six nodes. However, only five of them contribute to the phenotype and are active.
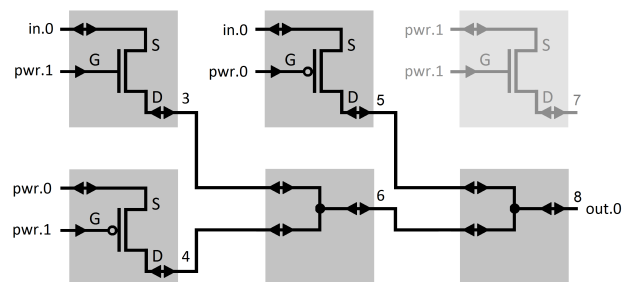

Fig. 2. Example of an encoded candidate circuit implementing *in.0/1* pass-logic polymorphic gate using three transistors. The circuit has one input (in.0), one output signal (out.0) and two power rails (pwr.0, pwr.1).

B. Evaluation of the candidate solutions

The goal of the evaluation is to determine whether the candidate circuit works correctly with regard to its functional description and whether the circuit meets other specified constrains. The evaluation of the candidate solution consists of two steps.

Firstly, set of active nodes is determined. Only the active nodes (nodes in a path from input nodes to outputs) represent the evaluated circuit. Inactive nodes are ignored. This operation is performed due to speed-up of the circuit simulation and because of skipping the short circuits in the unused part of the circuit. Then, multi-level discrete event-driven simulator is utilized to determine the circuit outputs for each input combination.

Quality of the candidate solution is determined by the *fitness function*, which compares the circuit outputs obtained from discrete simulation with the expected circuit outputs. If a short-circuit is detected for some input combination or a predefined number of simulation steps is reached, a penalty is subtracted from the total fitness value.

C. Search strategy

As a search algorithm, $1 + \lambda$ evolutionary strategy is utilized [9]. The initial population is generated in a random manner. Every new population consists of the best individual and λ offspring created using a point mutation operator which modifies randomly selected genes. The evolution is terminated when a predefined number of generations is reached.

As soon as a fully working solution is found, additional requirements (e.g. high input impedance) for circuit properties are checked. As soon as a fully working solution with all the desired properties is found, the circuit evolution continues in order to reduce the number of transistors being used.

Our simulations have revealed that some circuits designed by the original approach [12] do not have the intended behaviour. As an example, figure 3 depicts simulation results of four different $\overline{in_0}/xnor$ gates evolved by the mentioned approach, where the outputs of three such wrongly designed gates are shown.

Detailed analysis of the evolved circuits exposed an issue in the transistor model used in the discrete simulation. Specifically, the inaccuracy occurs when a discrete value denoted as 'Z' (high impedance) is present at transistor gate terminals for some combinations at the circuit input. Discrete simulation considered such a transistor as an open switch. However, the HSPICE simulation detected several transistors closed, probably because of charge remaining at their gates. In general, this issue can be fixed in different ways:

- More accurate discrete simulation with more complex transistor model can be implemented.
- Fast discrete simulation can be combined with the accurate HSPICE simulation done once per several thousands of generations.
- New constraint can be added to the circuit requirements, which ensures the 'Z' level will never be present at any transistor gate terminal at the end of discrete simulation.
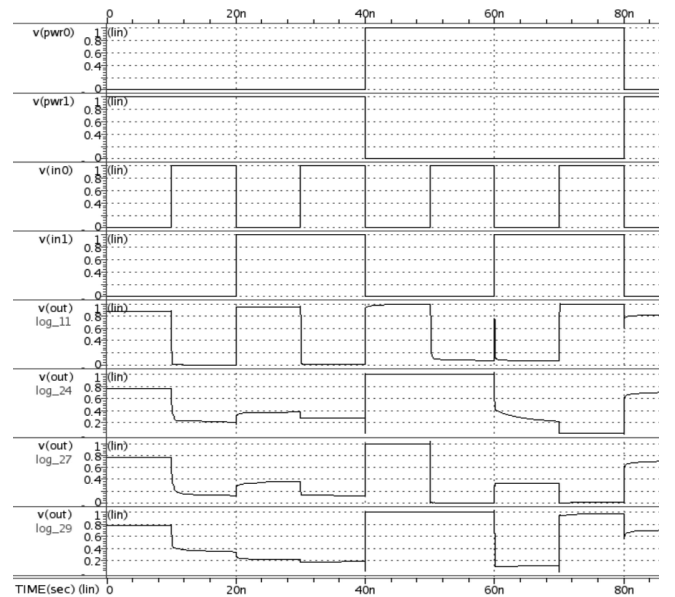

Fig. 3. HSPICE simulation results of four $\overline{in_0}/xnor$ polymorphic gates evolved by the approach presented in [12]. *log_24*, *log_27* and *log_29* circuits do not meet the expected behaviour.

As the first two approaches would extend the evolution time and/or increase required computing power, the third approach was utilized instead to produce valid polymorphic circuits in the context of this contribution.

D. Evolutionary optimization

The success rate of the evolutionary design decreases with growing number of constraints imposed on the gates. Figure 4 shows the success rate of 88 two-input polymorphic gates designed with the following evolution setup: CGP matrix size: 15x2, $\lambda = 4$, mutation: $3 \simeq 4\%$, number of generations: 2,000,000. With high input impedance constrain and prohibition of 'Z' level at transistor gates, the evolutionary approach was not able to design at about 14% circuits even after 1000 runs. Let us note that if any gate fulfilling all the requirements is found, the transistor count optimization is usually done just in tens of thousands generations.

To achieve a higher success rate of the gates evolved in Section IV, there was proposed the usage of an evolutionary optimization, which skips the difficult and, in a lot of cases, unsuccessful part of the evolutionary design. Before the evolutionary algorithm starts, one of the circuit candidates encodes the following circuit: Each polymorphic function is implemented by a conventional (non-polymorphic) CMOS circuit. These two circuits representing both polymorphic functions are switched by a multiplexer according to voltages on the power rails. Rest of the CGP elements encode just meaningless junctions.

As the encoded circuit meets both high input impedance and no 'Z' level at the transistor gates constrains, described improvements ensures 100% success rate. Let us note that the presented success rate is intended as a success rate of finding

TABLE I
SIZE OF THE SMALLEST FOUND SOLUTION OF MOSFET POLYMORPHIC GATES f_A/f_B WITH HIGH INPUT AND LOW OUTPUT IMPEDANCE

f_A		f_B															
		0	$\overline{a+b}$ nor	$\overline{a}b$	$\overline{a}$ not	$a\overline{b}$	$\overline{b}$ not	$a \oplus b$ xor	$\overline{ab}$ nand	ab and	$\overline{a \oplus b}$ xnor	b	$\overline{a}+b$	a	$a+\overline{b}$	$a+b$ or	1
0		0	5	5	3	5	3	7	5	7	8	4	6	4	6	6	0
$\overline{a+b}$	nor	5	4	6	6	6	6	9	8	9	7	6	4	6	4	7	5
$\overline{a}b$		5	6	4	6	8	6	6	4	7	9	6	7	6	7	6	6
$\overline{a}$	not	3	6	6	2	6	4	7	6	7	7	6	6	4	6	7	3
$a\overline{b}$		5	6	8	6	4	6	6	4	7	9	6	7	6	7	6	6
$\overline{b}$	not	3	6	6	4	6	2	7	6	7	7	4	6	6	6	7	3
$a \oplus b$	xor	7	9	6	7	6	7	6	7	9	9	8	9	8	9	8	8
$\overline{ab}$	nand	5	8	4	6	4	6	7	4	7	9	6	6	6	6	9	5
ab	and	7	9	7	7	7	7	9	7	6	8	6	6	6	6	8	6
$\overline{a \oplus b}$	xnor	8	7	9	7	9	7	9	9	8	6	8	6	8	6	9	7
b		4	6	6	6	6	4	8	6	6	8	4	6	6	6	6	4
$\overline{a}+b$		6	4	7	6	7	6	9	6	6	6	6	4	6	8	7	5
a		4	6	6	4	6	6	8	6	6	8	6	6	4	6	6	4
$a+\overline{b}$		6	4	7	6	7	6	9	6	6	6	6	8	6	4	7	5
$a+b$	or	6	7	6	7	6	7	8	9	8	9	6	7	6	7	6	7
1		0	5	6	3	6	3	8	5	6	7	4	5	4	5	7	0

Fig. 4. Success rate of polymorphic gates evolution design for different constraints imposed on the gates. X axis – number of successful evolution runs (out of 1000). Y axis – number of gates (88 total).

the behaviour of functional elements is controlled through swapping the power rail voltages, f_x/f_y polymorphic gate could be easily created from the f_y/f_x gate just by renaming its power supply inputs. Therefore, there is only 88 unique two-input gates.

The results were gathered from more than 5000 independent runs of evolutionary method for each polymorphic gate, as it is described in Section III. Both approaches comprising evolutionary design (sometimes produces more optimal circuit) and evolutionary optimization (each run produces a working circuit) were combined in order to get the most optimal gates. The results are based on the following experimental setup: CGP matrix size: 2x15 (design) or 1x50 (optimization), $\lambda = 4$, mutation: $3 \simeq 4\%$, number of generations: 2,000,000. Both high input impedance and no 'Z' level at transistor gates constrains were applied.

Due to the use of evolution optimization approach, all the 88 gates were successfully evolved. Table I shows the minimal number of transistors needed for implementation of the whole gate set, where the gray-backgrounded gates represent the unique (designed) gates. The other gates were easily derived from them. Just 6 transistors are sufficient for a single gate on average; most difficult gates require 9 transistors. Note that a/a and b/b gates consist of four transistors (two inverters) just because of the high input impedance requirement. They would be probably not used in the polymorphic circuit synthesis, similarly to $0/0$, $0/1$, $1/0$ and $1/1$ gates.

Let us show e.g. the $xor/\overline{a}b$ gate designed by 6 MOS transistors. The conventional xor gate with high input impedance consists of 8 transistors. Moreover, two inverters for the signal inputs are required. The conventional $\overline{a}b$ gate could be assembled with 4 transistors and one inverter. Considerable savings in the number of transistors are obvious. A $nand/nor$ gate, typical for polymorphic electronics, is designed by using 8 transistors. That is the same transistor count needed for

any gate with desired requirements, not success rate of finding the optimal gates (in number of transistors). Naturally, the second one is lower.

IV. DESIGNED POLYMORPHIC GATE SET

Main objective was to design a set of all two-input polymorphic gates with high input impedance, low output impedance and minimal number of transistors being used. The full set contains 256 two-input gates. However, large number of gates that belong into this set are similar and it is not necessary to explicitly design all of them.

Two circuits belong to the same P-class (are P-equivalent) if one of them can be derived from the other by permuting its signal inputs [13]. Without loss of generality it is sufficient to design only one polymorphic gate from each P-class. Other gates would be created just by permuting (i.e. renaming) signal inputs of the designed ones. Similarly, as it can be concluded from the principle of polymorphic electronics where

a separate implementation of both *nand* and *nor* gates in the convectional CMOS logic. The advantage of polymorphic approach *nand/nor* lies in the already implemented switch between these two functions, which comes as a natural built-in feature of such circuit component. In general, all the designed gates require significantly less transistors than a convectional circuit comprising two gates (implementing each function separately) and a multiplexer.

All the gates were successfully verified using HSPICE simulations and $45nm$ technology transistor models. Therefore, omission of the 'Z' level at transistor gates turned out to be acceptable. This observation is further supported by Figure 5 which shows HSPICE simulation results of four randomly selected $\overline{in_0}/xnor$ gates. Function of the polymorphic gates is changed every 40 ns – i.e. when the voltages on power rails are swapped.
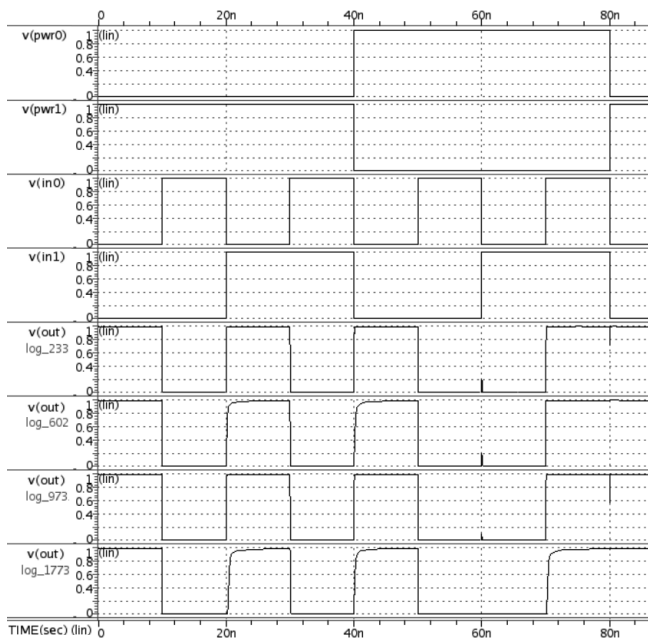
Fig. 5. HSPICE simulation results of four $\overline{in_0}/xnor$ polymorphic gates. Signal inputs are marked as in_0 and in_1, output as *out* and power rails are denoted as pwr_0 and pwr_1.

All the designed gates have high input impedance, low output impedance, short time of signal propagation (usually less than 1 ns), low power consumption and small number of transistors being used. Therefore, they meet all the requirements imposed on the ideal polymorphic gate.

V. CONCLUSION

A new approach to design of multifunctional digital circuits based on polymorphic electronics was proposed in this paper. MOS transistors are exploited in unconventional circuits where the circuit function is selected by mutual polarity of electric potentials on the power supply rails. In order to design new gates an evolutionary approach based on Cartesian genetic programming was utilized. The goal of the evolutionary algorithm was to minimize the overall number of transistors being used for each one of the evolved gates.

A complete set of two-input gates was designed. Functionality of all the gates was verified by HSPICE simulations. These gates show the best parameters of all previously published polymorphic gates – high input impedance and low output impedance, short time of signal propagation, low power consumption and small number of transistors being used.

This is the first complete set of polymorphic gates ever published. Wide range of proposed polymorphic gates (function combinations) may bring a significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size. Moreover, smaller parts of such designed circuits can be later optimized at the transistor level using proposed evolutionary optimization.

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Paper III

From Ambipolarity to Multifunctionality: Novel Library of Polymorphic Gates Using Double-Gate FETs

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From Ambipolarity to Multifunctionality: Novel Library of Polymorphic Gates Using Double-Gate FETs

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Abstract—**Ambipolarity, a unique feature typically found in some beyond silicon devices, e.g. CNT or organic FETs, is still treated today just as something rather peculiar. But in reality, it does not hinder such devices from utilization when it comes to the implementation of logic. From other point of view, this feature could be perceived as an opportunity to implement the logic in more refined and efficient way. The practical impact of ambipolarity results in devices which becomes more versatile than conventional FET element. In this paper, a set of multifunctional logic gates based on ambipolar FETs is presented. The multifunctionality of these gates means that each gate could exhibit one of two defined functions in a given moment. The selection of their function depends on circumstances under which the circuit is operated. The proposed set of gates could be employed in multifunctional circuits using techniques and procedures established for polymorphic electronics. This field of study, yet proposed nearly 20 years ago, now offers synthesis methods and application approaches to obtain an efficient implementation of more than one function in one logic circuit.**

Index Terms—**Polymorphic gate, ambipolar transistor, gate set, polymorphic electronics, digital circuit.**

I. Introduction

Last decade has witnessed a significant growth in research effort dedicated to the domain of so called post-silicon devices [1] or beyond CMOS (as discussed in ITRS since 2001) devices [2]. One of the key factors behind this endeavour is that wide range of innovative semiconductor materials (most of them based on an organic compound) with promising parameters have been developed. Another possible explanation of such course of events is given by the assumption that the end of the Moore's Law should be probably reached in just a few years [3], as it was already suggested by number of experts in the field. Such concern appears periodically since the invention of solid state semiconductor technology [4] and still prevails even after the introduction of the Moore's Law and CMOS technology.

However, due to the recent progress, there can be identified rich pool of devices with the potential to replace the contemporary silicon-based variants at a certain point. Moreover, the seemingly endless process of scaling down the dimensions of conventional silicon transistors (which was the main driver be-

hind keeping the pace with the Moore's Law up to the present time) is about to hit number of really serious challenges in connection with a chip design [5]. Some previously published works dealing with this topic indicate that future size reduction of conventional CMOS devices is going to become impractical or even physically unfeasible [6]. On the other hand, the exploitation of beyond silicon devices like carbon-nanotube [7], graphene [8] and silicon nanowires [9] based transistors, as well as organic single crystal [10] or heterostructures [11] ones, is considered by some researchers as a potential answer to a somewhat doubtful future of the Moore's Law.

In this context especially the end of Dennard Scaling paradigm (around 2006) shows that the way how to cope with today's issues of semiconductor industry may not reside only in bare scaling of semiconductor devices, but also in clever design process and utilization of logic. From this point of view, thoughtful strategy of employing certain unique features of beyond silicon devices within the target circuitry may also represent the way to accomplish more efficient implementation of the logic.

What should be intended by the more efficient implementation of the logic? Briefly, the objective here is to reduce the overall number of transistors necessary for implementation of a simple Boolean function (a logic gate), the number of transistors needed to implement a term of a logic function, etc. This feature is often called logic density. CMOS logic design seems to be almost perfect in that sense. In addition, fundamental CMOS logic structures are simple and reliable. During last several decades only minor improvement in the structure and implementation of basic logic gates has been achieved, and they are still used as fundamental blocks for all different types of digital devices. This is the best proof that those ones are very close to the optimal solution. But some recent works indicate that if some newly proposed devices are employed in a clever way, functional density of a typical CMOS circuit could be significantly improved [12], [13].

One of the remarkable ideas how to improve the logic density of a digital circuit involves the concept of so called Polymorphic electronics. This approach to the digital circuits design and implementation was proposed by the team of

A. Stoica at the NASA JPL nearly 20 years ago [14]. Fundamental idea behind the Polymorphic electronics paradigm is to obtain a single structure (circuit) which is able to execute more than one logic function. Of course, only one of those functions is actually realized by the circuit at a given moment. The decision which function is going to be selected depends on the actual circumstances of the circuit, on a state of the operating environment and, in general, on sensitivity of circuit structures to the occurrence of a particular phenomena with a direct impact on their electrical properties. Polymorphic circuits are built from polymorphic logic gates, the change of the function within the whole circuit is achieved through the change of Boolean functions exhibited by the individual instances of those polymorphic gates. Nevertheless, their mutual interconnection on a physical level remains unchanged.

From a brief description of the Polymorphic electronics conception provided above, it can be obviously concluded that the successful deployment of this circuit design paradigm is somewhat limited by the existence of an efficient implementation of suitable polymorphic gates. If those are designed and fabricated using standard CMOS-based technology (conceived primarily with the aim to ensure stable behaviour of logic gates, ergo not very suitable for polymorphic electronics implementation), the obtained results do not always achieve the desired efficiency [15], [16].

It seems that specific features of beyond silicon devices like ambipolarity may change the rules in the field of polymorphic electronics [17], [18]. In fact, ambipolarity allows to implement polymorphic gates by means of using so called ambipolar devices that have the intrinsic capability of changing their behaviour (e.g. conduction mode) even during runtime of the circuit. With the ambipolar property at hand, the idea of circuit polymorphism (as intended by Stoica [14] and his followers [16]) would be moved now towards more efficient (in terms of logic density) implementation of polymorphic circuits. This paper shows that almost any meaningful polymorphic logic gate (implementing two Boolean function in one circuit) could be implemented very efficiently using suitable "beyond CMOS" devices with the ambipolar capability. Such approach may contribute to the effort focused on improvement of logic density in the post-silicon era and maybe keep the Moore's Law alive.

The paper is organized as follows: Section II introduces the field of polymorphic electronics and various aspects related to the design of polymorphic gates. In Section III, double-gate ambipolar transistors, as a representative of promising beyond silicon devices, are shown. Section IV briefly describes an evolutionary approach used for design of new polymorphic gates. In Section V, two sets of designed gates based on double-gate ambipolar transistors are presented in details. Finally, Section VI provides a conclusion of this paper.

II. POLYMORPHIC ELECTRONICS

Polymorphic circuit represents specific type of a digital circuit that has the natural ability to perform two or more intentionally defined (logic) functions. The interconnections between individual components in such circuit remains unchanged on a physical level for all the permissible modes/functions. Unlike the conventional reconfiguration scheme that changes the actual circuit structure, the multifunctional nature of the polymorphic circuit is achieved due to the change of a behaviour within some of its components.

The mechanism how to swap the function may be carried out in various ways. It could be advantageous if a given component demonstrates its sensitivity to a specific phenomenon responsible for the function change. It turns out to be very useful if such phenomenon is inherently present in the circuit (like supply voltage level, temperature etc.). Then, the circuit changes its function in accordance with those circumstances and no special signal is needed to control this process. Such arrangement helps to keep the overhead paid for "extra" functions low.

The function change mechanism described above implies the existence of some application domains in which such kind of behaviour may help to get significant advantages. In general, these circuits could be used e.g. for:

- adaptation of the circuit behaviour to variable conditions with the target environment,
- reduction of power consumption or heat dissipation in order to preserve at least the essential circuit functionality, when energy goes low or temperature goes high,
- storing or hiding "extra" functions used as a watermark or other special features [14],
- embedded diagnostics purposes.

It is possible to recognize one important aspect shared within the application areas of polymorphic electronics suggested above: There typically exists so called primary function, which needs to be implemented first, and "additional" or "extra" function that might become desirable in some situations or under specific circumstances. Although the concept of polymorphic electronics generally admits several equally important functions implemented in one circuit, just one main and one or more auxiliary functions are considered due to practical reasons.

A. Polymorphic gates

Structure of a polymorphic circuit is typically analyzed on the gate level of abstraction. And exactly the gates themselves make the obvious difference between conventional logic and polymorphic circuits. Two main problems of the polymorphic electronics are:

1) The problem of suitable design (synthesis) methods for polymorphic circuits, i.e. how to map a description in the behavioural domain to a description in the structural domain. A lot of polymorphic circuits were designed using evolutionary-based methods, especially those involving Cartesian Genetic Programming [19]. But also non-evolutionary (conventional) design methods were proposed [20].

2) Search for suitable polymorphic components (gates). Implementation of the gate should be efficient (in terms of occupied chip area or transistor count).

The discovery of new gates suitable for a practical applications of polymorphic electronics have been reported very rarely during last decade. An attempt to develop a multifunctional gate using silicon MOS transistors mostly leads to a complicated structure with inferior parameters. On the contrary, new ambipolar devices hold a significant promise of developing new efficient and highly-refined gates with potentially very good electrical parameters.

Most of them are based on unconventional devices or technologies like organic ambipolar transistors [10], nanoelectronic structures [21], etc. These devices make it possible to accomplish the changes in behaviour of the circuit on a low levels within the design hierarchy – mostly related to the physical or material aspects. As it turns out, the research of polymorphic gates focused on the intrinsic ambipolarity feature of transistors as the way how to switch between two functions exhibited by the logic gate has the potential to enable highly efficient solution in comparison with the conventional MOS transistors employed previously.

Rich set of findings and observations gathered throughout numerous experiments with published polymorphic gates, as well as with in-house design of several novel polymorphic gates and practical experiments with applications of digital polymorphic electronics, have allowed to accurately formulate properties and criteria which should be fulfilled by ideal polymorphic gate:

1) high input resistance (the gate must avoid the excessive overloading of logic net generated by its inputs),
2) low output resistance (the aim is to achieve unambiguously defined logic levels at the gate and let them closely follow, if possible, the potential of supply source irrespective of the actual output load caused by subsequent logic net, whereby maintaining reasonable circuit noise immunity),
3) short time of signal propagation – definition based on measurement of transfer path delay between input and output ports (t_{pd}),
4) low power consumption,
5) small dimensions on a physical chip estate.

III. Ambipolar transistors

It has been already shown in various literature sources that many beyond silicon devices developed in recent years exhibit so called ambipolar behaviour. One of the most prominent examples in that context is obviously transistor as a switching element. The principle behind its ambipolar operation is that the transistor works exactly like P-type conventional MOS transistor under certain conditions, but for example a corresponding adjustment of gate bias triggers its transition into N-type mode – the transistor changes its behaviour and operates like N-type conventional MOS transistor. This behaviour seems to be very advantageous for complementary (CMOS like) structures, when it also creates the opportunity

to accomplish considerable simplification of the fabrication process – just one type of the transistor is used everywhere.
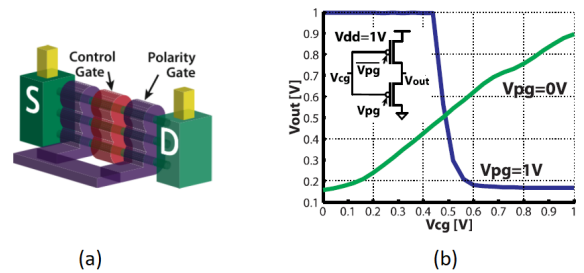

Fig. 1. (a) Stucture of SiNW ambipolar transistor from [22], (b) typical step response of ambipolar inverter designed with two identical transistors.

In this paper, multifuntional gates based on double-gate ambipolar FETs are presented. The operating mode of these transistors (P- or N-type) is determined by the second gate. Double-gate ambipolar FETs have been reported in emerging technologies such as carbon nanotubes (CNT) [7], graphene [23] and Silicon NanoWires (SiNWs) [22]. Figure 1 shows a scheme of such SiNW ambipolar transistor. The Control Gate (CG) works in the same way as in the case of standard unipolar FET, while the Polarity Gate (PG) controls the device conduction mode (polarity). For the utilization in polymorphic structures, the typical step response of ambipolar inverter formed by two such transistors is important. It is shown also in Figure 1, for v_{pg} connected to v_{dd} and $\overline{v_{pg}}$ connected to the ground. Due to the ambipolarity one transistor acts as a P-type transistor and the other as an N-type, although they are both manufactured as identical devices.
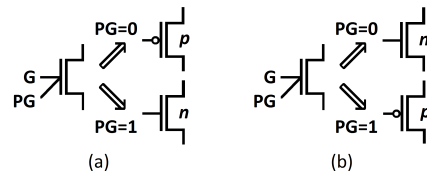

Fig. 2. Behaviour of ambipolar transistor (a) type 1, (b) type 2.

The behaviour of ambipolar transistors can be classified according to the selected technology [24], [25], which determines the actual behaviour through the dedicated control electrode. In general, those may fall into two different categories when it comes to the digital system design:

- **Type 1:** Ambipolar transistor acts as N-type in case of logic 1 at PG terminal and as P-type in case of logic 0 at PG terminal – Figure 2a.
- **Type 2:** Ambipolar transistor acts as P-type in case of logic 1 at PG terminal and as N-type in case of logic 0 at PG terminal – Figure 2b.

The observation that the polarity of ambipolar transistor is not specifically defined at an early stage by the fabrication process, but it could be also changed later on during its active operation, outlines the potential advantage that can be exploited during the development of polymorphic gates. Note that the inverter depicted in Figure 1 may exhibit the same

behaviour for both possible polarities of the power supply. This is because the inverter is symmetric and both transistors are the same. For non-symmetric and more complex gate structures (e.g. those aptly developed by an evolutionary algorithm) the behaviour should be apparently more interesting.

Rich set of digital circuits based on ambipolar transistors has already been published so far [25]. However, only few polymorphic circuits composed of these transistors and simultaneously controlled by swapping the potentials on the power supply rails were designed. Yang et al. presented NAND/NOR and XOR/XNOR gates [26]. Different implementations of XOR/XNOR and AND/OR gates for both ambipolar transistor types were published in [27].

IV. Approach to the gate design

In order to design new polymorphic gates, evolutionary approach proposed earlier in [28] was further refined and used in the context of this contribution. To achieve a fast simulation run with reasonable accuracy, a discrete simulator with switch-level transistor model extended by a threshold drop degradation effect is utilized.

The approach is capable of designing circuits with high input impedance and low output impedance. The resulting circuits are optimized with regard to the overall number of transistors being used. As all the transistors in gates designed by this approach work in saturation mode, low power consumption in general is also expected. Let us notice that these characteristics correspond to the requested properties and criteria for polymorphic circuit from Section II.

One of the key prerequisites for implementation of any Boolean function is the availability of a Boolean constant in the circuit. Normally, this requirement is fulfilled implicitly by the presence of power supply rails. But what is the constant in the circuits where voltages on power supply rails could be swapped mutually?

Some gates proposed in this paper require a Boolean constant connected inside its structure. Therefore, although two supply wires are enough for this type of polymorphic electronics, the voltage needs to be rectified internally. The actual way of rectification would be usually application- and chip-specific. However, in the vast majority of the polymorphic circuits designed so far, polymorphic gates are combined with the conventional gates. Therefore, Boolean constants are already present in the circuit and no rectifier is needed.

Note that the Boolean constants are not required in all designed gates – just the power supply rails are sufficient e.g. for $\overline{a}b/\overline{a}+b$ gates shown in Figure 6 and Figure 7.

A. Circuit representation

Evolutionary approach for polymorphic circuits design at the transistor level requires a convenient representation. Such representation needs to have a capability of encoding bidirectional graph structures including junctions. We utilized Cartesian genetic programming (CGP) proposed by J. Miller [19].

The proposed representation is derived from the usual CGP representation of gate-level circuits. Each candidate circuit is represented using two-dimensional array of nodes where each dimension has a fixed size. It allows the usage of encoding with fixed-length array of integers (so called chromosome) containing function of the nodes and their interconnection. Each node consists of three input terminals and one output terminal. Furthermore, it can act as an ambipolar transistor or a junction. Ambipolar transistor uses all three input terminals, whereas the junction only two of them. The utilized nodes are depicted in Figure 3. Input terminals of each node can be independently connected to the output terminal of any node placed in previous columns or to one of the primary circuit inputs.
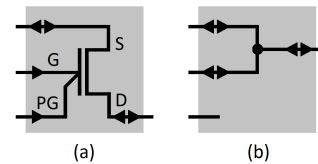

Fig. 3. CGP nodes: (a) ambipolar transistor and (b) junction. The arrows denote the possible directions of signal flow which have to be considered during the circuit evaluation.

The junction nodes couple three wires (two input and one output) together. As a consequence of that, loops and multiple connections are natively supported.

Figure 4 demonstrates the principle of selected encoding on a polymorphic inverter ($\overline{in}/\overline{in}$ gate, also shown in Figure 1) which inverts the logical value of input signal independently of the mutual polarity between power supply rails. The example of chromosome encodes a candidate circuit using four nodes. However, only three of them contribute to the phenotype and are active.
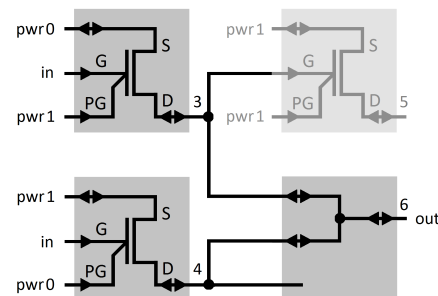

Fig. 4. Example of an encoded candidate circuit implementing polymorphic inverter using two ambipolar transistors of type 1. The circuit has one input (in), one output signal (out) and two power supply rails (pwr_0, pwr_1).

B. Ambipolar transistor model

A fast simulator is needed to enable the evolutionary design method to sufficiently explore the search space. However, reasonable accuracy is required for design of the circuits that will work in a real environment. In order to meet these criteria, a discrete simulator employing the switch-level transistor model (abstracted from dynamic parameters such as

power consumption or signal propagation delay) was utilized. In addition, this model considers also the threshold drop degradation effect.

Despite the fact that the domain of double-gate ambipolar transistors has been exposed to the attention of scientific community for several years now, there still do not exist any freely available, exact models which could be used in a combination with advanced circuit simulation tool kits like HSPICE. Therefore, it was necessary to create a discrete model of ambipolar transistor (for both type 1 and type 2 variants), matching the functionality outlined in Section III, more general.

The proposed model is based on six discrete values (voltage levels): logic 0 (denoted as '0'), logic 1 ('1'), degraded 0 ('L'), degraded 1 ('H'), high impedance ('Z') and undefined value ('X'). This specific approach results in design of circuits, where either '0' or '1' is always present at all terminals of each transistor in the circuit. The advantage of using degraded values in the model lies in the design of non-conventional circuits where the degraded and non-degraded values (e.g. '1' and 'H') could be combined in a junction, with a non-degraded value ('1') as a result. That can be useful in some designed circuits in order to reduce their size.

C. Evaluation of the candidate solutions

The goal of the evaluation is to determine whether the candidate circuit works correctly with regard to its functional description and whether the circuit meets other specified constrains. The evaluation of the candidate solution consists of two steps.

Firstly, set of active nodes is determined. Only the active nodes (nodes in a path from input nodes to outputs) represent the evaluated circuit. Inactive nodes are ignored in order to speed-up of the circuit simulation and in order to skip the short circuits in the unused parts of the circuit. Then, discrete event-driven simulator is utilized to determine the circuit outputs for each input combination.

Quality of the candidate solution is determined by the fitness function, which compares the circuit outputs obtained from the simulation with the expected circuit outputs. If a short-circuit is detected for some input combination or a predefined number of simulation steps is reached, a penalty is subtracted from the total fitness value.

D. Search strategy

As a search algorithm, $1 + \lambda$ evolutionary strategy is utilized [19]. The initial population is generated in a random manner. Every new population consists of the best individual and λ offsprings created using a point mutation operator which modifies randomly selected integers in the encoded circuit. The evolution is terminated when a predefined number of generations is reached.

As soon as a fully working solution is found, additional requirements (e.g. high input impedance, no 'Z' voltage level at CG pin, etc.) for circuit properties are checked. When a fully working solution with all the desired properties is evolved, the

circuit evolution continues in order to reduce the number of transistors being used.

E. Evolutionary optimization

As the evolutionary algorithms are based on the heuristic search of state space, success of the evolutionary design is not guaranteed. Moreover, the success rate significantly decreases with growing number of constraints imposed on the gates. Figure 5 shows the success rate of 88 two-input polymorphic gates designed with the following evolution setup: CGP matrix size: 10x2, $\lambda = 4$, mutation: $3 \simeq 4\%$, number of generations: 4,000,000. With high input impedance constrain and prohibition of 'Z' level at transistor gates, the evolutionary approach was not able to design at about 70% circuits even after 1000 runs. Let us note that if any gate fulfilling all the requirements is found, the transistor count optimization is usually done just in thousands or in tens of thousands generations.
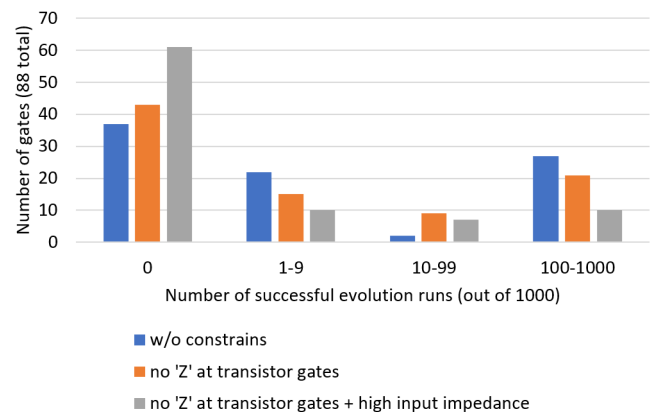

Fig. 5. Success rate of polymorphic gates evolution design for different constraints imposed on the gates.

To achieve a higher success rate of the circuit design, we propose to use an evolutionary optimization, which skips the most difficult and, in a lot of cases, unsuccessful part of the evolutionary design. Before the evolutionary algorithm starts, one of the circuit candidates encodes the following circuit: Each polymorphic function is implemented by a conventional (non-polymorphic) CMOS circuit. Outputs of these two circuits are connected to a multiplexer which selects one of them according to voltages on the power supply rails. The rest of CGP elements encodes just meaningless junctions.

As such encoded circuit meets all the required constrains imposed on the designed gate (high input impedance, non-degraded voltage levels on each circuit node for each input, etc.), the design approach is used just for optimization of a working circuit. Therefore, each run of evolutionary algorithm produces a working circuit. Let us note that the presented success rate is intended as a success rate of finding any gate with desired requirements, not success rate of finding the optimal gates (in number of transistors). Naturally, the second one would be lower.

TABLE I
Size of the smallest found solution of polymorphic gates f_A/f_B with high input and low output impedance utilizing type 1 ambipolar transistors

f_A		f_B															
		0	$\overline{a+b}$	$\overline{a}b$	$\overline{a}$	$a\overline{b}$	$\overline{b}$	$a\oplus b$	$\overline{ab}$	ab	$\overline{a\oplus b}$	b	$\overline{a}+b$	a	$a+\overline{b}$	$a+b$	1
			nor		not		not	xor	nand	and	xnor					or	
0		0	5	7	3	7	3	8	5	7	8	5	7	5	7	7	0
$\overline{a+b}$	nor	5	4	8	6	8	6	9	4	9	9	9	8	9	8	8	5
$\overline{a}b$		7	8	6	7	9	9	9	8	10	11	8	6	11	10	8	7
$\overline{a}$	not	3	6	7	2	9	6	9	6	8	9	10	7	6	9	8	3
$a\overline{b}$		7	8	9	9	6	7	9	8	10	11	11	10	8	6	8	7
$\overline{b}$	not	3	6	9	6	7	2	9	6	8	9	6	9	10	7	8	3
$a\oplus b$	xor	8	9	9	9	9	9	8	9	11	8	9	10	9	10	10	8
$\overline{ab}$	nand	5	4	8	6	8	6	9	4	8	9	9	8	9	8	9	5
ab	and	7	9	10	8	10	8	11	8	6	10	8	8	8	8	6	7
$\overline{a\oplus b}$	xnor	8	9	11	9	11	9	8	9	10	8	9	10	9	10	10	8
b		5	9	8	10	11	6	9	9	8	9	4	8	8	11	8	5
$\overline{a}+b$		7	8	6	7	10	9	10	8	8	10	8	6	11	9	10	7
a		5	9	11	6	8	10	9	9	8	9	8	11	4	8	8	5
$a+\overline{b}$		7	8	10	9	6	7	10	8	8	10	11	9	8	6	10	7
$a+b$	or	7	8	8	8	8	8	10	9	6	10	8	10	8	10	6	7
1		0	5	7	3	7	3	8	5	7	8	5	7	5	7	7	0

V. Sets of designed polymorphic gates

Main objective was to design a complete set of two-input polymorphic gates for each type of double-gate ambipolar transistor presented in Section III where the function performed by the gate is selected according to the mutual polarity of the power supply rails. These gates exhibit high input impedance, low output impedance and minimal number of transistors being used. Each complete set contains 256 two-input gates. However, each set contains large number of mutually similar gates and it is not necessary to explicitly design all of them.

Two circuits belong to the same P-class (are P-equivalent) if one of them can be derived from the other by permuting its signal inputs [29]. Without the loss of generality it is sufficient to design only one polymorphic gate from each P-class. Other gates would be created just by permuting (i.e. renaming) signal inputs of the designed ones. Similarly, as it can be concluded from the principle of polymorphic electronics where the behaviour of functional elements is controlled through swapping the power rail voltages, f_x/f_y polymorphic gate could be easily created from the f_y/f_x gate just by renaming its power supply inputs. Therefore, there is only 88 unique two-input gates.

The results were gathered from more than 3000 independent runs of evolutionary method for each polymorphic gate, as it is described in Section IV. Both approaches comprising evolutionary design (sometimes produces more optimal circuit) and evolutionary optimization (each run produces a working circuit) were combined in order to get the most optimal gates. The obtained results are based on the following experimental setup, which turned out to be the most suitable for this specific task: CGP matrix size: 2x12 (design) or 1x45 (optimization), $\lambda = 4$, mutation: $3 \simeq 4\%$, number of generations: 10,000,000. High input impedance constrain was
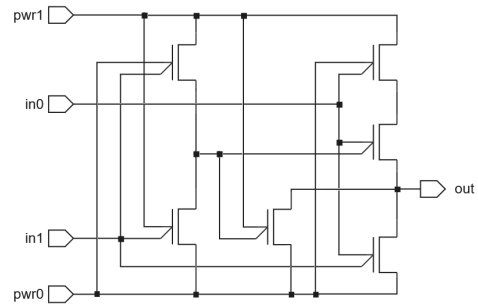

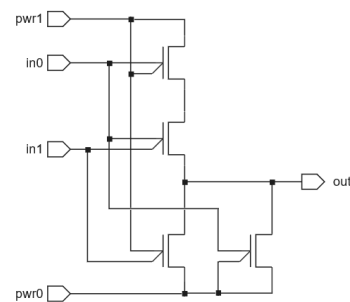Fig. 6. Polymorphic $\overline{a}b/\overline{a}+b$ gate using ambipolar transistors of type 1.

Fig. 7. Polymorphic $\overline{a}b/\overline{a}+b$ gate using ambipolar transistors of type 2.

applied as well as constrains ensuring non-degraded values (i.e. either logic 0 or logic 1) at all wires inside the gate for each input.

Due to combination of evolutionary design and evolution optimization approaches, all 88 unique gates were successfully evolved for each set of gates. The other gates were easily derived from them. Table I shows the minimal number of type 1 ambipolar transistors needed for implementation of the whole gate set. A single gate requires 7.7 transistors on average; most difficult gates are composed of 11 transistors. Note that a/a

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TABLE II
SIZE OF THE SMALLEST FOUND SOLUTION OF POLYMORPHIC GATES f_A/f_B WITH HIGH INPUT AND LOW OUTPUT IMPEDANCE UTILIZING TYPE 2 AMBIPOLAR TRANSISTORS

f_A		f_B															
		0	$\overline{a+b}$ nor	$\overline{a}b$	$\overline{a}$ not	$a\overline{b}$	$\overline{b}$ not	$a\oplus b$ xor	$\overline{ab}$ nand	ab and	$\overline{a\oplus b}$ xnor	b	$\overline{a}+b$	a	$a+\overline{b}$	$a+b$ or	1
0		0	5	5	3	5	3	6	5	7	6	3	5	3	5	5	0
$\overline{a+b}$	nor	5	4	6	6	6	6	8	4	7	8	7	6	7	6	8	5
$\overline{a}b$		5	6	4	6	7	7	9	6	6	9	6	4	7	7	6	5
$\overline{a}$	not	3	6	6	2	7	6	8	6	7	8	6	6	4	7	8	3
$a\overline{b}$		5	6	7	7	4	6	9	6	6	9	7	7	6	4	6	5
$\overline{b}$	not	3	6	7	6	6	2	8	6	7	8	4	7	8	6	8	3
$a\oplus b$	xor	6	8	9	8	9	8	6	8	8	9	8	9	8	9	8	6
$\overline{ab}$	nand	5	4	6	6	6	6	8	4	8	8	7	6	7	6	7	5
ab	and	7	7	6	7	6	7	8	8	4	8	6	6	6	6	4	7
$\overline{a\oplus b}$	xnor	6	8	9	8	9	8	9	8	8	6	8	9	8	9	8	6
b		3	7	6	8	7	4	8	7	6	8	2	6	8	7	6	3
$\overline{a}+b$		5	6	4	6	7	7	9	6	6	9	6	4	7	7	6	5
a		3	7	7	4	6	8	8	7	6	8	8	7	2	6	6	3
$a+\overline{b}$		5	6	7	7	4	6	9	6	6	9	7	7	6	4	6	5
$a+b$	or	5	8	6	8	6	8	8	7	4	8	6	6	6	6	4	7
1		0	5	5	3	5	3	6	5	7	6	3	5	3	5	7	0

and b/b gates consist of four transistors (two inverters) just because of the high input impedance requirement. They would be probably not used in the polymorphic circuit synthesis, similarly to 0/0, 0/1, 1/0 and 1/1 gates.

Table II shows the minimal transistor count for the same gate set when the gates are assembled from ambipolar transistors of type 2. As it is obvious from the table, usage of type 2 ambipolar transistors results in much smaller circuits in terms of their size. Just 6.2 transistors are sufficient for a single gate on average, while the most difficult gate requires only 9 transistors.

Let us show e.g. the $\overline{a}b/\overline{a}+b$ gate designed by 6 ambipolar transistors of type 1 (Figure 6) or by 4 transistors of type 2 (Figure 7). The conventional $\overline{a}b$ gate with high input impedance consists of 6 MOSFET transistors. The same number of MOSFET transistors is also required by conventional $\overline{a}+b$ gate. Considerable savings in the transistor count are obvious. The polymorphic gate implements two functions (instead of one) while using the same number or even less transistors.

Another gate, $\overline{a}/a+b$ (NOT/OR), is comprising just 8 transistors. That is the same transistor count needed for a separate implementation of both NOT and OR gates in the convectional CMOS logic. The advantage of polymorphic NOT/OR gate lies in the already implemented switch between these two functions, which comes as a intrinsically built-in feature of such circuit component. In general, all the designed gates require significantly less transistors than a conventional circuit comprising two gates (implementing each function separately) and a multiplexer.

As it was mentioned before, there do not exist any freely available exact models of double-gate ambipolar transistors. A simplified behavioural HSPICE model was implemented to verify the gate outputs for all the presented gates. As
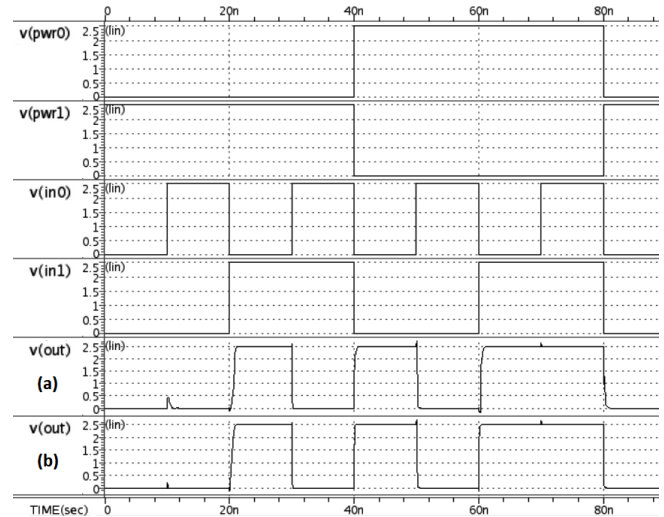

Fig. 8. Simulation results of $\overline{a}b/\overline{a}+b$ polymorphic gates from (a) Figure 6 and (b) Figure 7.

the simulation model has a rather general nature, it does not reflect e.g. delay, threshold drop degradation effect or power consumption of any specific ambipolar transistor. Figure 8 shows the simulation results of $\overline{a}b/\overline{a}+b$ gates depicted in Figure 6 and Figure 7. Function of the polymorphic gates is changed every 40 ns – i.e. when potentials on the power supply rails are swapped.

All the designed gates exhibit high input impedance, low output impedance and small number of transistors being used. Due to the selected design approach and the fact that all transistors in the presented gates work in the saturation mode, low power consumption (in terms of existing polymorphic circuits) is also expected. Therefore, no requirement imposed on the ideal polymorphic gate (summarized in Section II) is

violated. Specific power consumption and signal propagation delay of the gates depends on the particular ambipolar transistor technology the gate set is implemented with.

When designing a more complex polymorphic circuit, pass-logic type of gates is also acceptable in some parts of the circuit. Similarly to the sets of gates presented above, sets of pass-logic gates for both type of ambipolar transistors were also designed. Usage of these gates can save up to 4 transistors per gate (1.0 transistor in average) in case of type 1 ambipolar transistors and also up to 4 transistors per gate (0.6 transistor in average) in case of type 2 ambipolar transistors.

VI. CONCLUSION

A huge number of multifunctional digital gates based on polymorphic electronics was proposed in this paper. Ambipolar transistors are exploited in unconventional circuits where the function performed by the circuit is selected according to the mutual polarity of the power supply rails. In order to design new gates an evolutionary approach based on Cartesian genetic programming was utilized. The goal of the evolutionary algorithm was to minimize the overall number of transistors being used for each one of the evolved gates.

Two complete sets of two-input polymorphic gates were designed. These gates exhibit the properties required for the ideal polymorphic gates – high input impedance, low output impedance, low power consumption and small number of transistors being used. Moreover, another two sets with pass-logic polymorphic gates were proposed in order to reduce the size of more complex polymorphic circuits. Functionality of all the gates was verified by HSPICE simulations.

These sets are the first complete sets of polymorphic gates based on ambipolar transistors ever published. Wide range of efficient polymorphic gates may bring a significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size. Moreover, the existence of complete two-input gate sets may also open the path to the creation of new synthesis methods, which are expected to deliver more efficient results than the existing ones in terms of target circuit size or the overall synthesis runtime.

ACKNOWLEDGMENT

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Paper IV

PoLibSi: Path Towards Intrinsically Reconfigurable Components

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PoLibSi: Path Towards Intrinsically Reconfigurable Components

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Abstract—**One of the main research directions of polymorphic electronics is focused on various issues connected with the design of basic polymorphic components – polymorphic gates. Without a sufficient amount of polymorphic gates offering good properties, conventional electronics will be most likely the preferred way before polymorphic electronics in application scenarios targeting multifunctional behaviour or reconfiguration. The main objective of this paper is to propose a library called PoLibSi which contains eight sets of efficient bi-functional two-input polymorphic gates, whose function is selected by mutual polarity of dedicated power rails. The gate sets differ in the transistor type (conventional MOSFET, emerging double-gate ambipolar transistors), feature the gate sets were optimized to (transistor count, delay, power consumption) and input impedance constraint. The individual gates were designed by means of using an evolutionary based approach and further validated by HSPICE simulations. Each gate implementation includes a schematic, HSPICE description and simulation results. Moreover, propagation delay and power consumption is provided for all MOSFET based gates. Furthermore, each gate set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Besides providing polymorphic gates with better properties to the research society, the aim of the proposed library is to improve the synthesis of polymorphic circuits in terms of the resulting size, as it is also shown in the paper. Finally, the PoLibSi library is available at: www.fit.vutbr.cz/~inevoral/polibsi***

Index Terms—**Polymorphic gate, bi-functional gate, gate set, MOSFET, ambipolar transistor, polymorphic electronics.**

I. INTRODUCTION

The area of digital circuits design has experienced an extremely vivid development during several previous decades. Although the first physical implementation of CMOS-based logic circuit has been successfully demonstrated more than 55 years ago [1], this technology still prevails as the major choice even in case of the cutting-edge electronic devices. However, the contemporary state-of-the-art paradigms, design flows and fabrication procedures are getting closer to the ultimate technological constraints. A specific approach how to address those challenges, at least in certain situations, could be based upon the principles of so-called polymorphic or multifunctional electronics with the intrinsic reconfiguration capabilities.

Arrival of polymorphic electronics in 2001, which was introduced by A. Stoica and his research group in NASA Jet Propulsion Laboratory, has opened the path towards design and implementation of multifunctional digital circuits [2]. Main idea behind the polymorphic electronics approach is connected with a circuit structure that is able to perform more than one intended function. It is characteristic that the interconnection of the circuit components (gates) remains unchanged in contrast to the conventional electronics where the function must be explicitly hard-wired.

Traditional method of reconfiguration involves certain overhead in both space and time domain [3]. On the other hand, polymorphic circuits typically have no such drawback (the function change is immediate) [4] and, moreover, overhead in the size domain is mostly smaller than for a classic reconfiguration, which typically involves downloading of a dedicated bitstream into the target reconfigurable platform. This is given by the fact that structure comprising a lot of switches or multiplexers is typically needed for reconfiguration purposes, as well as corresponding memory resources for storing the configurations. Neither additional memory nor dedicated reconfigurable structure pattern is needed for polymorphic electronics. If the synthesis of a polymorphic circuit is performed cleverly, the cost paid for an additional function could be very low [5].

One of the main issues behind the adoption of this approach is given by the analogue nature of the circuit function change itself. It consequently leads to rather analogue design concepts projected into the polymorphic gates rather than staying in purely digital domain. The result is that some transistors work in a linear mode or short power supply. During recent years various research activities have been focused on the utilization of so called post-silicon devices [6] for the construction of polymorphic circuit elements. It seems that some features of post-silicon devices, like the ambipolar charge carrier conductivity, may play an important role in the field of polymorphic electronics. Such ambipolar transistors have been reported in emerging technologies such as carbon nanotubes (CNT) [7], graphene [8] and silicon nanowires (SiNWs) [9], [10]. The change of polymorphic gate function based on ambipolarity suggest the opportunity to achieve very efficient and neat implementation of logic gates [11] due to fully digital implementation – transistors operate as switches in the saturation mode.

The reason why the creation of multifunctional or poly-

morphic gates based on exploitation of purely digital design techniques has been considered difficult and rather unfeasible approach lies in the fact that conventional MOS transistors, when used as switches, are very stable devices. Thus, an attempt to develop a multifunctional gate using silicon MOS transistors was mostly leading to a complicated structure with inferior parameters. However, an innovative approach how to surmount these challenges has been proposed in [12]. It virtually opened a way towards the construction of a complex library comprising digital logic gates with intrinsic reconfiguration capabilities.

The structure of the paper is organized as follows: Brief introduction to fundamental aspects of polymorphic electronics is given in Section II. Then, Section III contains review of existing polymorphic gates. Main objective of this article, i.e. proposal of a complex library that contains digital logic gates designed according to the procedures reported in [11] and [12], is presented together with its thorough discussion in Section IV. Finally, conclusion and future outlooks can be found in Section V.

II. POLYMORPHIC ELECTRONICS

Polymorphic electronics can be characterized as relatively new discipline in the field of digital circuits and systems. Its notion depicts a group of digital circuits that have the ability to perform more than one function, while the wiring of a given circuit keeps still the same layout in all the intended operating modes. Selection of the corresponding function, which the circuit is going to execute, simply depends on the actual state of the target operating environment. Most importantly, the change of the polymorphic circuit function comes into the effect right away (without any eminent delay perceived) and sensitivity to the environments is naturally embedded into the circuit itself [2].

It is important to emphasize at this point that all the required circuit functions are designed in a fully intentional manner rather than, for example, as a specific fault condition caused by exceeding certain operating parameters of the circuit. State of the environment, where such circuitry is going to be deployed, can be accurately expressed through a physical quantity with a direct impact on the electrical properties of circuit building elements. Then, it is possible to clearly determine the actual function to be realized by that circuit according to the specific value of a relevant parameter [13]. Such behaviour is useful for circuits that must adapt themselves to unfriendly environment, e.g. by imposing restriction of power consumption [14].

A. Components for polymorphic electronics

Utilization of the polymorphic electronics concept, and therefore construction of more complex circuit arrangements, is somewhat limited by the availability of suitable polymorphic gates. In fact, only two of the polymorphic gates have been physically fabricated so far. The other polymorphic gates reported in literature were either only simulated or tested in a FPTA [15]. For instance, the 6-transistor NAND/NOR gate controlled by V_{dd} was fabricated in a 0.5-micron HP

technology [16]. Another NAND/NOR gate controlled by V_{dd} was introduced in [17] (Figure 1). Significant extent of deploying modified CMOS-based technology is rather symptomatic for practically of all such examples. However, an innovative approach using conventional n-/p-channel MOSFET transistors as the principal elements of digital logic gates has been recently published [12].
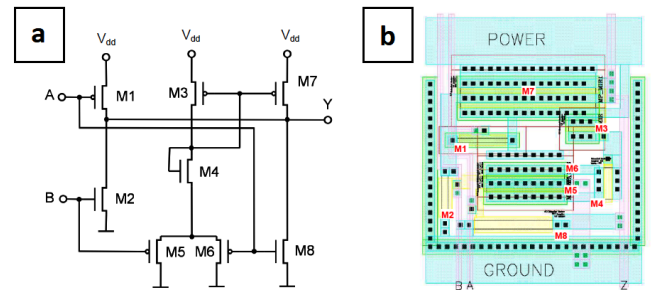

Fig. 1. Internal structure of polymorphic NAND/NOR gate on a transistor level (a) and its corresponding physical layout using standard CMOS AMIS 0.7 um technological library (b). The resulting size of a single gate (b) is approximately 55.8 um x 68.2 um [17].

However, the domain of polymorphic electronics doesn't have to be unnecessarily restricted to the design effort carried out exclusively on the transistor level. There have been already reported numerous research activities where the objective was to create even some larger circuit structures exhibiting multifunctional behaviour, while preserving the fundamental principles of polymorphic electronics paradigm. Such example, where circuit blocks like 8-bit min/max, min/add and similar ones were successfully conceived, can be found in [18].

B. Existing application scenarios

Despite the objection that polymorphic electronics might be often deemed nothing more substantial than a bare peculiarity within the realm of digital circuits, it is indeed possible to demonstrate its natural benefits and advantages through a number of various application scenarios that have been previously addressed. For example, let us consider the following situations when physically fabricated platform REPOMO32 [19], which contains an array of polymorphic and CMOS-based digital circuit elements, was utilized in order to implement the required multifunctional behaviour:

1) Polymorphic FIR signal filter [20].
2) Transition function of cellular automaton [21].
3) Safety and fault tolerant systems [17], [22].
4) Security measures physically unclonable functions [23].

One of the possible scenarios for the practical exploitation of polymorphic circuits suggested above refers to the domain of cellular automata. It represents a computational paradigm involving a set of mutually interconnected cells (circuits blocks) that can perform various operations and transition between permissible states. Multifunctional circuitry adopting the principles of polymorphic electronics provides a way towards an efficient implementation of such functionality on
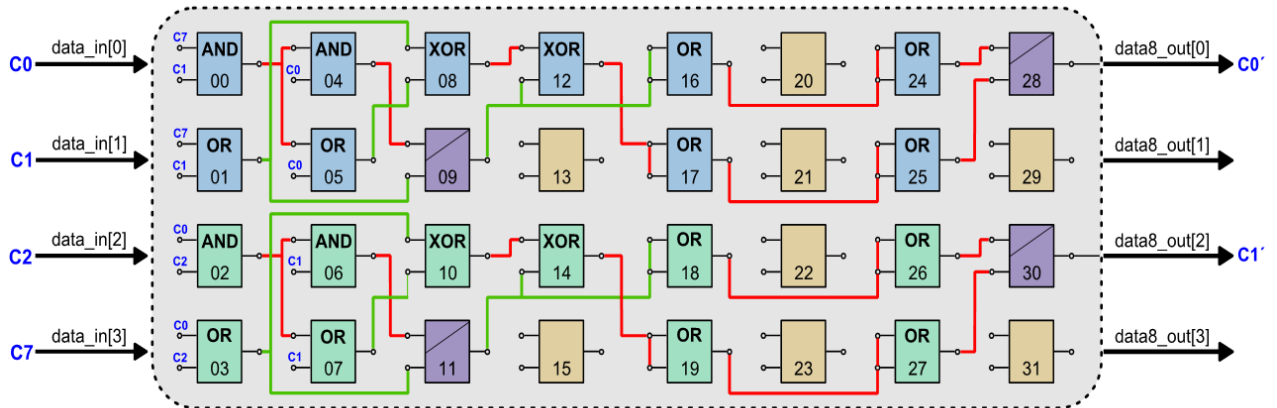
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Fig. 2. Internal configuration of REPOMO32 chip depicting the gate-level implementation of rule number 150 (3-bit parity) in the first mode and rule number 232 (3-bit majority) in the second mode. Two independent cells of cellular automaton are shown in the picture. Polymorphic NAND/NOR gates are depicted as violet blocks. Closer details can be found in [21].

the circuit level. Possible approach to that problem using polymorphic electronics and, in particular, reconfigurable chip REPOMO32, was demonstrated in [21]. The details of transitional function implementation are shown in Figure 2. The advantage in this case is given by the fact that it is not necessary to implement both transitional functions (i.e. 150/232) separately and switch their output accordingly by an additional multiplexer. Instead of that, just one multifunctional circuit block is designed and the particular function is enabled due to an intrinsic reconfiguration feature related to the specified variation of power supply voltage level.

C. Open issues of polymorphic electronics

Some of the most important problems of polymorphic electronics, which deserve further attention in order to be resolved or further improved from the current level of advancement, are especially the following ones. The 1st issue is obviously connected with the effort to provide suitable polymorphic components (gates). As it was demonstrated above their availability is rather limited, when only few types have been physically fabricated. The 2nd aspect is the problem of an appropriate design and synthesis methods for polymorphic circuits. One of the most common approaches of polymorphic circuits design is based on using some evolutionary methods. Finally, the 3rd problem is focused on identification of appropriate classes of applications, where the polymorphic electronics could deliver an advantage in contrast to conventional solutions.

This paper deals with the 1st mentioned issue – design of the polymorphic gates.

III. POLYMORPHIC GATES

Since the emergence of polymorphic electronics, about twenty polymorphic gates have been reported in the literature. Let us note that most of them employs the conventional MOSFET transistors. Such gates are summarized in Table I, where logic functions performed by the gates are given together with

recommended setting of the control signal variable. Size of the gates could be determined from the number of transistors only approximately (transistors occupy different areas, gates were fabricated using different fabrication technology, etc.).

TABLE I
A SURVEY OF EXISTING SILICON-BASED CMOS POLYMPORPHIC GATES.

Functions	Controlled by	Control value	Transistor count	Ref.
AND/OR	V_{dd}	1.2/3.3 V	8	[16]
NAND/NOR	V_{dd}	3.3/1.8 V	6	[24]
NAND/NOR	V_{dd}	3.3/1.8 V	10	[25]
NAND/NOR	V_{dd}	5/3.3 V	8	[17]
AND/OR	temperature	27/125 °C	6	[2]
AND/OR	temperature	5/90 °C	8	[2]
NAND/NOR	temperature	80/120 °C	12	[13]
AND/OR	ext. voltage	0/3.3 V	6	[2]
AND/OR/XOR	ext. voltage	3.3/1.5/0 V	9	[2]
NAND/NOR	ext. voltage	0/5 V	10	[26]
NAND/NOR	ext. voltage	0/5 V	10	[27]
NAND/NOR	ext. voltage	5/0 V	8	[28]
NAND/NOR	ext. voltage	5/0 V	10	[28]
NAND/XOR	ext. voltage	5/0 V	9	[28]
NAND/WIRE/AND	ext. voltage	0/1/-1.8 V	9	[29]
XNOR/XOR	ext. voltage	5/0 V	16	[30]

Large number of these gates do not obviously meet reasonable parameters. As a result of that, perspective of their utilization for real applications becomes rather bleak. For example gates controlled by the power supply level were designed as analog circuits which led to higher power consumption (static current up to 120 μA [17]), higher propagation delay (few tens of μs [24]) and/or larger area of occupied chip estate (size of the transistors differs up to ten times [17]).

The behaviour of gates controlled by the temperature is usually stable only in specified intervals of this quantity. If

the temperature doesn't change fast (and it usually doesn't), circuit composed of temperature controlled components can perform an unspecified function for a relatively long time.

Several gates based on different emerging devices (especially ambipolar transistors) were published later [31] [32]. Their function depends on polarity of power supply voltage – i.e. the second circuit function is available when the electric potentials of the power supply rails are swapped.

Research experiences gathered throughout numerous experiments with published polymorphic gates, as well as with in-house design of several novel polymorphic gates and practice with applications of digital polymorphic electronics, have allowed to define properties and criteria which should be fulfilled by polymorphic gate:

1) high input resistance (the gate must avoid an excessive load applied to the preceding logic net caused by its inputs),
2) low output resistance (the aim is to achieve unambiguously defined logic levels at the gate output irrespective of a given output load caused by subsequent logic net),
3) short time of signal propagation,
4) low power consumption,
5) small dimensions.

It was shown that it is possible to successfully meet these criteria with gates whose function depends on mutual polarity of two dedicated power rails [11] [12]. This concept leads to simple gates based on a digital design where transistors work in the saturation mode. Such gates are close to the conventional CMOS circuits in terms of their features, structure and design constraints. Note that some gates require also the conventional v_{ss} and v_{dd} power rails with stable potentials in order to ensure the proper functionality and computationally complete logic of the concept.

An extensive library of gates based on the concept outlined above is introduced in the following chapter. Conventional MOSFET transistors together with double-gate ambipolar transistors were chosen as target technologies.

IV. PoLibSi Library

The PoLibSi library (www.fit.vutbr.cz/~inevoral/polibsi) is a freely available library comprising more than 38,000 bi-functional two-input logic gates, whose function is selectable via mutual polarity of two dedicated power rails. For the sake of clarity, all those gates are arranged into particular gate sets according to the transistor type (MOSFET, double-gate ambipolar), feature the gates were optimized to (transistor count, delay, power consumption) and other relevant properties (e.g. input impedance constraint) as Table II shows.

Each gate set is complete, i.e. provides at least one transistor-level implementation (but usually even other distinct variants) of each possible function that a bi-functional gate can execute. A conventional (mono-functional) two-input gate can have one of 16 Boolean functions (0, a, $a + b$, ab, etc.). Therefore, a complete set of bi-functional two-input gates contains 256 various combinations ($0/a$, $0/a + b$, $a + b/ab$, etc.). However, a large number of these 256 combinations

TABLE II
LIST OF DESIGNED GATE SETS. DIFFERENCES BETWEEN TYPE 1 AND TYPE 2 AMBIPOLAR TRANSISTOR ARE DESCRIBED IN [11]. SETS MARKED BY AN ASTERISK (*) ARE CURRENTLY UNDER CONSTRUCTION.

Gate set name	Transistor type	High input impedance	Optim. criteria
MOS_SIZE_HI	MOSFET	yes	size
MOS_DELAY_HI	MOSFET	yes	delay
MOS_POWER_HI*	MOSFET	yes	power
MOS_OPT_HI*	MOSFET	yes	power, delay
AMBI_N1_HI	ambipolar, type 1	yes	size
AMBI_N1_NO	ambipolar, type 1	no	size
AMBI_P2_HI	ambipolar, type 2	yes	size
AMBI_P2_NO	ambipolar, type 2	no	size

are similar enough and it is not necessary to attend all of them. Without the loss of generality, it is sufficient to design only 88 unique combinations for each gate set [11], [12]. The remaining 168 gates can be easily derived from those 88 just by mutual swapping their power signals or input signals names (P-equivalence) in the schematic – e.g. $\overline{b}/b$ gate can be created from $\overline{a}/a$ gate just by renaming signal a to b. PoLibSi is interactive and provides guidelines to the user how to create the rest of gates from the designed ones.

Unique transistor-level implementations of each polymorphic function (function combination) in each gate set were obtained from more than 5000 independent runs of evolutionary-based methods described in [11] and [12]. Only the resulting circuits with minimal number of transistors/delay/power consumption became part of PoLibSi. Moreover, mutual comparison of those implementations made it possible to exclude the identical or highly similar instances. Gates were considered as equivalent when:

- two transistors connected in series (between the same junctions) were swapped and/or:
- drain and source terminals in the same transistor were swapped and/or:
- gate and polarity gate terminals in the same transistor were swapped (applies only to ambipolar transistors of Type 1) and/or:
- compared circuits are equivalent after mutual renaming of a and b circuit inputs (applies only for f_1/f_2 gates where $f_1, f_2 \in \{0, 1, and, or, nand, nor, xor, xnor\}$)

Each gate implementation in the PoLibSi library has been evaluated using HSPICE simulation. In case of MOSFET based gates, 45nm BSIM4 transistor models V1.0 from [33] were utilized. Substrates of all n-MOS transistors were connected to v_{ss} and substrates of all p-MOS transistors were connected to v_{dd}. Power supply voltage ($|v_{dd}| - |v_{ss}|$) was set according to the recommendation for this type of models to 1 V [34]. For the simulation purposes, output of the gates was connected as an input of inverter loaded by 1 pF capacitor. Two separate HSPICE simulations were performed for each MOSFET based gate. A basic one shows gate output for each circuit input. The other one is depicting in details transitions

between all possible pairs of circuit inputs, which allowed to assess a propagation delay value of each gate and to compute the average power consumption. Note that 10 ns after change of inputs, output of all presented gates reached at least 0.95 V when logic 1 was expected and at most 0.05 V when logic 0 was expected.

Although the field of double-gate ambipolar transistors has been continuously explored for several years now, there still do not exist any freely available, accurate models which could be used in a conjunction with HSPICE simulator. Thus, accurate propagation delay and power consumption were not expressed for any specific target technology. In order to validate at least the gate outputs for each circuit input, a simplified behavioural model consisting of 8 conventional MOSFET transistors (see Figure 3) was involved to emulate the behaviour of double-gate ambipolar transistors. As this model has a rather general nature, it does not reflect e.g. delay, threshold drop degradation effect or power consumption of any specific ambipolar transistor.
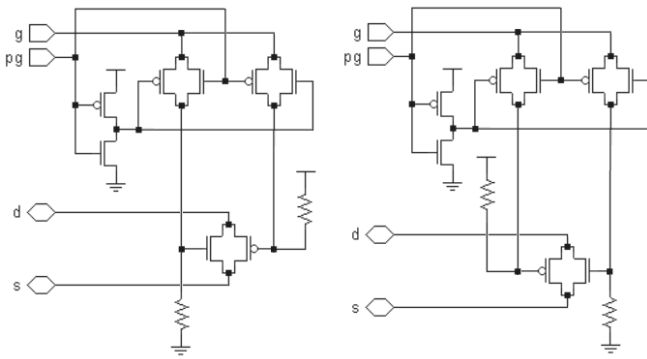
Fig. 3. Behavioural model of double-gate ambipolar transistor of Type 1 (left) and Type 2 (right) used in simulations performed throughout this contribution.

The PoLibSi library provides HSPICE description, schematics and simulation results for all designed gate implementations included within MOSFET gate sets. In case of gate sets based on ambipolar transistors, the design approach found hundreds or even thousands of different implementations of several polymorphic functions. In order to make the library compact, HSPICE description, schematics and simulation results are shown for at most 10 unique implementations of each gate. HSPICE descriptions of the rest unique gates are then accessible via a .zip compressed file.

As an example from the PoLibSi library, NOT/XNOR gate with identifier *f1700* out of the MOS_DELAY_HI gate set was chosen. The gate is depicted in Figure 4, HSPICE description follows in Listing 1. Input signals are denoted a and b, power signals influencing the circuit behavior $pwr0$ and $pwr1$ and the output is denoted out. As the transistor-level digram of that particular gate shows, it also contains v_{ss} and v_{dd} – power signals which do not change their potentials.

Figure 5 shows the simulation of the gate. Every 10 ns, there is a new combination of circuit inputs. When $pwr0 = 0$, the circuit performs NOT function ($\overline{a}$), otherwise it behaves as
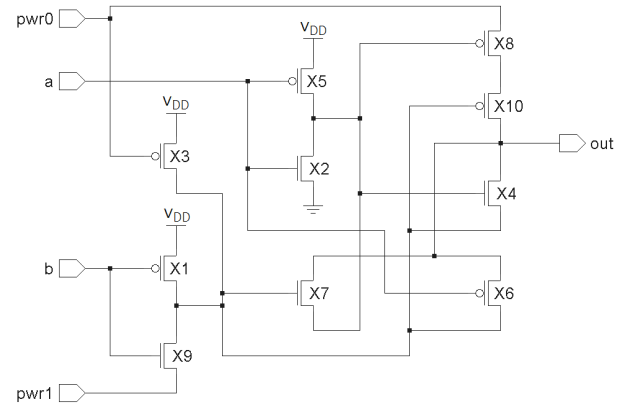
Fig. 4. Schematic of #f1700 NOT/XNOR gate from MOS_DELAY_HI gate set.

XNOR ($\overline{a \oplus b}$). Simulation results were utilized for calculation of non-functional properties: Maximal propagation delay of this gate is 34 ps and average power consumption 384 nW.

```
*X source gate drain n/pMOS
X1 vdd b J6 pMOS
X2 vss a J0 nMOS
X3 vdd pwr0 J6 pMOS
X4 J6 J0 out nMOS
X5 vdd a J0 pMOS
X6 out a J6 pMOS
X7 J0 J6 out nMOS
X8 pwr0 J0 B16 pMOS
X9 pwr1 b J6 nMOS
X10 B16 J6 out pMOS
```

Listing 1. Example of HSPICE description derived for #f1700 NOT/XNOR gate from MOS_DELAY_HI gate set.
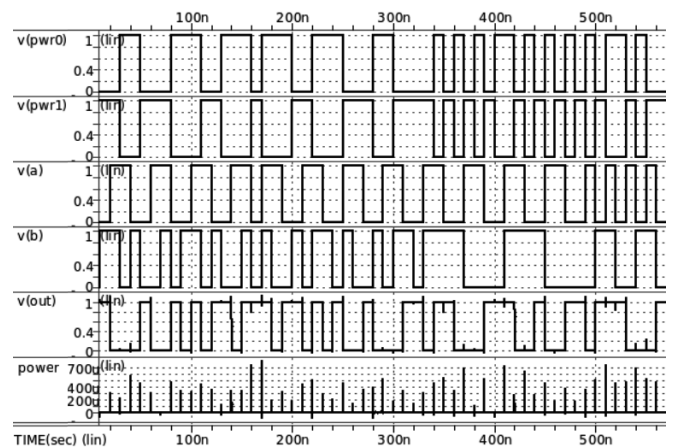
Fig. 5. HSPICE simulation of #f1700 NOT/XNOR gate (depicted in Figure 4) with use of 45nm transistor model. Grid size is 0.2 V resp. 100 μW in Y-axis.

In order to get also real measurement results, the same gate was assembled with ALD1103PBL, ALD1106PBL and ALD1107PBL – ICs with N- and P-channel MOSFET transistors. The measurement results for power supply of 2.5 V are depicted in Figure 6. Signal *a* had a square-like waveform with frequency of 307 kHz, i.e. gates inputs were changed with the frequency around 614 kHz. It is important to point out that this measurement was done just as an interesting addition to this paper. In addition, it is necessary to take into account that each gate optimized on the layout level will achieve significantly different properties than a gate assembled using the breadboard approach.
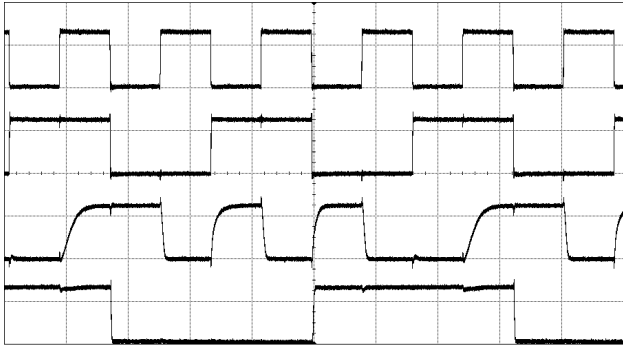
Fig. 6. Measurement of NOT/XNOR gate (depicted in Figure 4) with use of real transistors. Signal order is (from the top): *a*, *b*, *out* and *pwr*0. Signal *pwr*1 always had negated logic value of *pwr*0 signal. Grid size is 2 V in Y-axis and 2 μs in X-axis.

In terms of the total transistors count, power consumption and delay, properties of the described gate (#f1700) are competitive to separate (parallel) implementations of NOT and XNOR functions in 45nm CMOS technology [33]. In fact, comparing sizes of gates directly on the transistor level without the consideration of physical layout related aspects is always very intricate. The NOT/XNOR gate (#f1700) presented above consists of 10 transistors. However, MOS_SIZE_HI gate set provides also two variants of NOT/XNOR gates (#a558 and #a738) composed of only 7 transistors. In general, all bi-functional gates in PoLibSi require less number of transistors than separate (parallel) implementations of their functions followed by a multiplexer. Furthermore, most of the gates optimized to the size require equal or less number of transistors than just separate implementations of their functions.

In order to show the space-efficiency of designed bi-functional gates, AMBI_N1_HI, AMBI_P2_HI and MOS_SIZE_HI gate sets were utilized for design of three more complex bi-functional circuits (RTL components), each with two 8-bit input operands and one 8-bit output. Their functions were chosen according to Sekanina [18], who designed them (also with regards to the circuit size) with a combination of conventional mono-functional gates and NAND/NOR gate, so far typical approach to polymorphic circuits implementation.

Table III compares implementations of these circuits across the technologies. As Sekanina determines cost of the circuits

in relative area, a ratio of 1:4 (4 transistors match one area unit) was set. That keeps 1 area unit cost of NAND and NOR gates, which are implemented same or similar in all compared technologies. Although the comparison ratio is approximate only, the results show that circuits synthesized with use of PoLibSi gates occupy significantly smaller relative area.

V. Conclusion

One of the main research directions of polymorphic electronics is focused on various issues connected with the design of basic polymorphic components – polymorphic gates. Without a sufficient amount of polymorphic gates with good properties, conventional electronics will be most likely the preferred way before polymorphic electronics in application scenarios targeting multifunctional behaviour or a reconfiguration.

Main objective of this paper was to introduce a freely available library of efficient polymorphic gates, whose parameters are distinctly better than parameters of polymorphic gates published earlier. This new generation of gates is based on both conventional MOSFET and emerging double-gate ambipolar transistors. The gates were designed by means of using an evolutionary based approach and further validated by HSPICE simulator. They are classified into the gate sets according to the utilized transistor type, feature the gates were optimized to (size, delay, power consumption) and input and output impedance constraints. Each gate implementation comprises a schematic, HSPICE description and simulation results. Moreover, propagation delay and power consumption (in 45nm technology) is provided for all MOSFET based gates.

Gate sets in the library provide efficient implementations of all possible functions that a two-input bi-functional gate can execute. Therefore, it is supposed that their utilization in synthesis process of more complex bi-functional circuits could make these circuits also adequately effective, as design of three RTL components in the last chapter of this paper indicates. Those components were more efficient than previous implementations with polymorphic gates in terms of the overall circuit size.

Despite relatively large number of multifunctional gates included in the proposed library, there still exist plenty of opportunities for additional improvements or extensions. For example, gates in PoLibSi were designed using discrete transistor models presented in [35]. The library can be further extended by usage of modern transistor types (FinFET, FDSOI, etc.) if their behaviour corresponds to the mentioned models or if similar models of their behaviour will be created.

The ambipolar technology holds an unquestionable perspective of using just one type of transistor which is capable of making the transition between n-/p-channel modes as needed in a given circuit structure. The current version of the library contains gate sets based on double-gate ambipolar transistors. It could be interesting to create a separate gate set also for three-terminal ambipolar transistors, because less terminals count lead to a simplified interconnection scheme on a physical level.

TABLE III

IMPLEMENTATION COST OF 8-BIT RTL COMPONENTS PUBLISHED IN [18] AND RTL COMPONENTS DESIGNED BY GATE SETS FROM POLIBSI LIBRARY.

Function	MOSFET [18]		MOS_SIZE_HI			AMBI_N1_HI			AMBI_P2_HI		
	Gates	Area	Transistors	Gates	Area	Transistors	Gates	Area	Transistors	Gates	Area
ident/min	50	68.3	203	51	50.8	234	51	58.5	204	51	51.0
min/max	74	86.3	224	52	56.0	230	53	57.5	202	51	50.5
or/max	64	90.3	216	50	54.0	230	52	57.5	200	50	50.0

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Paper V

Efficient Implementation of Bi-functional RTL Components – Case Study

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Efficient Implementation of Bi-functional RTL Components – Case Study

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Abstract—**The emergence of highly optimized implementations of many bi-functional gates allows an efficient implementation of components at a higher level of abstraction. In several classes of applications which typically involve RT level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at RT level a skilled designer is still able to design a far more complex circuits by himself. If a set of efficient bi-functional RTL components is available, their utilization is expected to improve efficiency of the resulting circuit. In this paper, validity of this assumption is demonstrated through a design of bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/subtractor circuit was created and optimised. This circuit was subsequently utilised for design of multi-bit adder/subtractor which was successfully simulated at the transistor level with MOSFET implementation of bi-functional logic gates. Besides adder/subtractor, an increment/decrement RTL component is also presented.**

Index Terms—**Multifunctional electronics, bi-functional RTL component, bi-functional gate, full adder/subtractor, half adder/subtractor, increment/decrement.**

I. INTRODUCTION

Recent years bring a high amount of research papers, in which some multifunctional components for digital circuits are presented. Most of them report such kind of components, that could be utilised on the gate level. The term "multi-functionality" here means that the circuit is able to perform different logic functions under different circumstances. These circumstances can be induced intentionally, i.e. the function, performed by the circuit at particular moment, can be undoubtedly chosen.

Motivations for such kind of research are various. Some researchers try to utilise features of some beyond silicon technologies [1] [2], some researchers demonstrates advantages of evolutionary design of digital circuits [3] [4]. Either bottom-up or top-down approach is chosen by authors, in almost all cases, the main advantage of such kind of design is more efficient implementation of several functions by one compact circuit. In certain class of applications, this approach is more efficient than conventional reconfiguration [5], which is today the first choice for implementation of multifunctional devices. The price paid for this efficiency is lower flexibility. Prevailing part of the circuit has fixed functionality, the same for all functions or modes of the circuit. Only small parts of the circuit (few components) change their behaviour. If the conventional reconfiguration would be used for such kind of application, a lot of overhead is needed to implement and maintain the reconfiguration, whereas small modifications or changes are needed. Moreover, the change of function in case of reconfiguration needs some time to be performed. In contrary, multifunctional circuits change their functions immediately [6].

It is typical for most applications that two different functions alternate. One of them is typically the "main" function and the second one is "auxiliary". For example, it may be some diagnostic mode or a special mode in which a test could be applied more easily than in normal mode of operation. Another possible application is implementation of some low-power or emergency mode in which the function of the circuit is restricted but most important actions are maintained [7] [8]. However, there is no reason why both (or all) alternative functions could not be of equivalent significance.

Wide range of applications utilising multifunctional components is designed at the gate level. It means that multifunctional components are logic gates and to obtain the circuit, some suitable logic synthesis method is needed [9]. Logic synthesis of multifunctional digital circuits is very challenging and most of the existing circuits were synthesized using evolutionary design. However, there are some applications, where the design can be executed on higher level of abstraction than the gate level. For example applications where rather arithmetic than pure logic operations take place (e.g. filters for image and video processing) [10]. Such design could be done on RT level. Then, multifunctional RTL components are needed. Moreover, the design at this level of abstraction should be easier and further modification towards multifunctionality could be done in most cases by hand. Such approach helps to avoid complicated process of multifunctional digital circuit synthesis.

The paper is organized as follows: Section II introduces the field of bi-functional logic gates and circumstances controlling their function. Section III shows several bi-functional arithmetic circuits designed from the bi-functional gates. Section IV deals with design of RTL component, which is able to add signed numbers in the first mode and to subtract them in the other one. Section V provides a conclusion of this paper.

II. Bi-functional logic gates

There are different approaches how to change a function of a circuit. The function just performed by the circuit can be determined by a supply voltage level [11], an external signal [12], a temperature of the chip [13] or even by its illumination. The behaviour of gates controlled by a non-electric quantity (last two mentioned approaches) is usually determined only in specified intervals of this quantity. If the change of this quantity value is not fast (and it is usually not fast), the circuit can perform an unspecified function for a relatively long time. Therefore, these approaches haven't had any practical use yet.

The multi-functional (polymorphic) gates were often designed with ability to change their functions according to the power supply voltage level because the power supply is connected to all parts of the circuit. There is no need to use any other signal leading to all multifunctional gates, which will transmit information about their current function. The disadvantage of such multifunctional gates, originally proposed by A. Stoica [3], lies in rather complicated analog design of these gates and in non-optimal parameters of such gates, whether it is power consumption, speed (propagation delay of the gates) or area occupied in the chip.

In recent years, we proposed a concept of bi-functional gates whose behaviour depends on the polarity of supply voltage [14]. More accurately, the second circuit function is available when the electric potentials on the power supply rails are swapped. This concept leads to simple gates based on a digital design where each transistor works in saturation mode (in comparison to the gates controlled by the supply voltage level). Therefore, such gates are close to the conventional CMOS gates in terms of their design constraints, structure and features. At the same time, they offer an efficient implementation of two Boolean functions in one gate. Moreover, such gates keep the properties of a concept, where information about the current circuit function is distributed via power supply rails.

We designed three complete sets of bi-functional two-input gates (each set is composed of 256 gates) controlled by the polarity of supply voltage. One set of the gates is based on MOSFET transistors [14], the others are based on different types of ambipolar transistors [15]. All these gates exhibit high input and low output impedance, low power consumption and finally, they were optimised to small number of transistors being used.

III. Bi-functional arithmetic circuits

As it was stated in Section I, there are some applications, where the design can be executed on higher level of abstraction than on the gate level. For example applications where rather arithmetic than pure logic operations take place (e.g. digital filters). Such design could be done on RT level and requires RTL components. In this chapter, bi-functional arithmetic components based on bi-functional gates are proposed.

A. Increment/Decrement

Zebulum et al. proposed a multifunctional ripple counter, which could be able to reset its value and to count in both up and down directions [16]. The counter was built on multifunctional JK flip-flops, but has never been fabricated or even simulated. As this proposal was based on polymorphic NAND/NOR/AND gates controlled by analog voltage on external signal, the electric properties of such counter (e.g. power supply current) would probably avoid its deployment in the real applications.

To achieve an up- and down- counter with better parameters, conventional D flip-flops can be utilised in cooperation with bi-functional combination circuits, which generate the incremented or decremented value.

Such increment/decrement circuit can be assembled with use of the bi-functional gates very easy. LSB bit of such number must be always negated. The upper bites need to be adjusted by eventually carry/borrow bit generated from less significant bits. The most efficient implementation in terms of the gate number is shown in Figure 1. As LSB circuit block requires different functionality than the others, two circuit blocks were designed. Each of them is composed of two gates only.
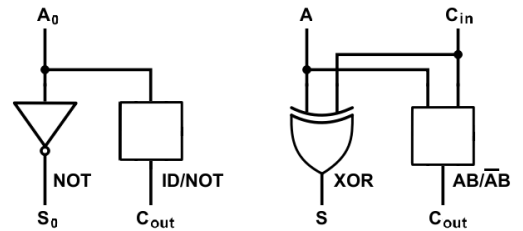

Fig. 1. Schematic of bi-functional increment/decrement circuit blocks: LSB block (left), block for more significant bits (right).

B. Adder/Subtractor

Increment/decrement block (depicted on the right of Figure 1) is a circuit comprising functions of a half adder and a half subtractor – just C_{in} input would be renamed to B in the conventional notation. Such circuit implements arithmetic operation $S = A + B$ in the first mode and $S = A - B$ in the other one, whereas C_{out} is the output carry (resp. borrow bit in the subtractor mode).

A bi-functional operator exhibiting behaviour of both a full adder and a full subtractor expects $S = A + B + C_{in}$ function in the first mode and $S = A - B - C_{in}$ in the other one. At the logic level, the outputs of full adder can be described by well-known formulas:

$$S = A \oplus B \oplus C_{in}$$
$$C_{out} = AB + AC_{in} + BC_{in}$$

where $\oplus$ marks exclusive OR. The outputs of a subtractor are described by following formulas:

$$S = A \oplus B \oplus C_{in}$$
$$C_{out} = \overline{A}B + \overline{A}C_{in} + BC_{in}$$

As it is obvious from the formulas above, the bi-functional full adder/subtractor circuit can be easily assembled by 7 gates – two conventional XOR gates, two OR gates, one AND gate and two bi-functional gates implementing $ab/\overline{a}b$ functions.

In order to get the most efficient implementation of this circuit by using up to 256 different bi-functional gates, an evolutionary approach to the circuit design at the gate level was utilised. The resulting circuit was optimised with regards to minimal number of gates being used.

Figure 2 shows one of the best circuits designed by the evolutionary algorithm. It consists of three conventional and two bi-functional gates only. The depicted circuit also consist of the lowest number of MOSFET transistors (24 transistors) among the designed circuits when the MOSFET bi-functional gate set [14] is used for implementation of the circuit at the transistor level.
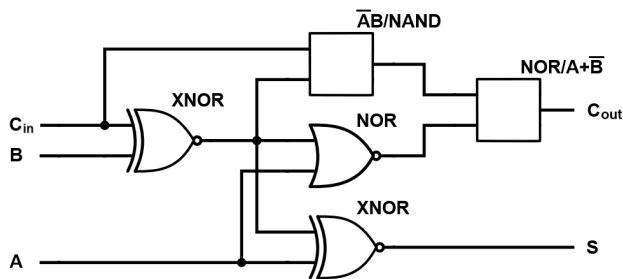

Fig. 2. Schematic of one-bit full adder/subtractor bi-functional circuit at the gate level.

IV. CASE STUDY – ADDER/SUBTRACTOR

At the RT level, n-bit arithmetic units are often needed. A typical and mostly employed arithmetic unit is n-bit adder or subtractor. Such kind of RT-level components could be employed e.g. in signal filters [10] and in a wide range of similar signal processing circuits. Because signal processing is a domain where precision depends on amount of resources (besides the power) and on the other hand, less precise (or more approximated) result is better than no result, multifunctionality or polymorphism of the implementation that allow reduction of power consumption is welcome [8].

For the purpose of addition and subtraction of unsigned numbers, the cascade of one-bit adder/subtractor blocks proposed in Section III can be used without any limitation. Similarly to the conventional full adder circuit, proposed block can be used also to add and to subtract signed numbers encoded by two's complement. In this case, exclusive OR (XOR gate) of two most significant C_{out} outputs of the adder/subtractor cascade must be used in order to get the valid overflow flag of the whole adder/subtractor cascade.

We utilised the evolutionary algorithm mentioned above also to optimise the MSB adder/subtractor block in the cascade in order to avoid any external XOR gate. Such designed circuit (simultaneously optimised to minimal number of gates and minimal number transistors as well) is shown in Figure 3.

It consists of three conventional gates and one bi-functional gate. An implementation by the MOSFET bi-functional gate set consist of 24 transistors.
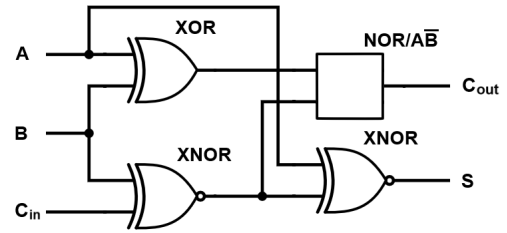

Fig. 3. Schematic of MSB full adder/subtractor block determined for unsigned numbers encoded by two's complement.

In order to show the functionality of such designed solution comprising (at different level of abstraction) bi-functional gates and bi-functional one-bit adder/subtractor blocks, we simulated a three-bit adder/subtractor circuit. It consists of two blocks depicted in Figure 2 and MSB block depicted in Figure 3 assembled in a cascade. As a target technology, MOSFET bi-functional gate set [14] together with 45nm n-MOS and p-MOS transistor models [17] and power supply of 1V was chosen.

Figure 4 shows the simulation results of such created bi-functional circuit for $c_{in} = 0$. Every 5 ns, there is a new combination of operand values. Input signals a_2, a_1, a_0 represent operand A. Similarly, signals b_2, b_1, b_0 represent input operand B and signals s_2, s_1, s_0 represent output S. Signals a_0, b_0 and s_0 are LSB. Function of the circuit is changed every 320 ns – i.e. when potentials on pwr_0 and pwr_1 rails are swapped. When $pwr_0 = 0$, the circuit function performs an addition ($S = A + B$), otherwise the circuit function is subtraction ($S = A - B$). Output c_{out} signalizes overflow.

As an example, lets show 195-200 nanosecond timeslot from the simulation, where the circuit performs an addition. Input operands are $A = -4$ (binary 100) and $B = -1$ (111) at the selected timeslot. As the resulting number (-5; 1011 binary) is out of the range of values, which the three-bit two's complement representation is able to encode, the overflow output signal (c_{out}) is set. The resulting output $S = 3$ (011) also correspond to the LSB bits of expected value -5 (1011).

Simulation of the 3-bit adder/subtractor circuit was successful for all input values, also for $c_{in} = 1$. Maximal propagation delay – found just during change of the arithmetic functions – is less than 0.5 ns.

V. CONCLUSION

Thanks to the existence of libraries with efficient implementations of all two-input bi-functional gates, it is possible to effectively implement also the bi-functional RTL components. In several class of applications, typically signal processing, which allow a design at RT level, these components can circumvent various issues related to synthesis of multifunctional
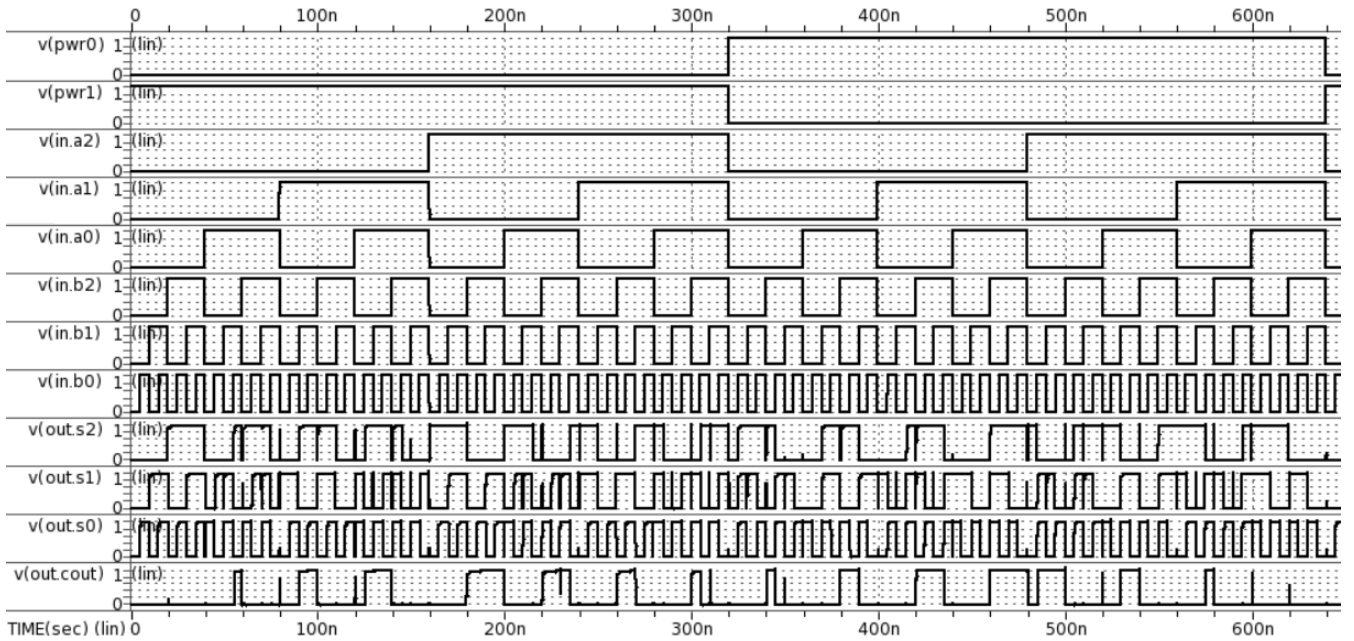
Fig. 4. Simulation results of a three bit adder/subtractor circuit with $c_{in} = 0$ which is composed of two blocks depicted in Figure 2 and MSB block depicted in Figure 3 connected to the cascade.

circuits at the gate level. While the synthesis at the gate level is challenging and researchers have still been dealing with problem of efficient synthesis methods, a skilled designer is able to design a lot of more complex circuits at RT level by himself. If the designer has a set of efficient implementations of RTL components, the resulting circuit would be also adequately efficient.

Validity of this assumption was demonstrated through an example with bi-functional adder/subtractor circuit. At the gate level, one-bit adder/subtractor circuit was assembled and optimised. This circuit was utilised for design of multi-bit adder/subtractor which was successfully simulated at the transistor level with MOSFET implementation of bi-functional logic gates.

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