Supervisor assessment of Master's Thesis

Student: Vávra Jan, Bc.
Title: Graphical Simulator of Superscalar Processors (id 21991)
Supervisor: Jaroš Jiří, doc. Ing., Ph.D., DCSY FIT BUT

1. **Assignment comments**
   The goal of this Master's thesis was to develop a complex graphical simulator of a superscalar possessor which would be configurable, and would allow to execute user defined programs and follow particular phases of their execution. **The outcome of this work is an impressive piece of software** consisting of over 20 thousands lines of java code illustrating the operation of a fully configurable out-of-order superscalar processor based on the RISC-V instruction set. The simulator will become a welcome tool in the Computation Systems Architectures course and a platform for implementation additional components such as cache memories. Although the simulator has a few minor imperfections, **I am really enthused by this outcome.**
2. **Literature usage**
   The student worked mostly independently with related literature, actively looked up information on existing simulators, current processor architectures and algorithms used. From my perspective, the student has a deep knowledge in this area and used the literature appropriately.
3. **Assignment activity, consultation, communication**
   The student was very active, dutiful and diligent during the whole year. The meetings were organised biweekly and took about one hour. The student was always well-prepared being able to present his progress in details and draw future work directions. He was open to new ideas and willing to devote much effort in the implementation and testing. He developed a very good project strategy right after the project had been started, and was following the set timeline till the very end. The progress of the work is captured by a GitLab repository with more than 90 commits. I must praise him for a professional structure of the repository with several branches, issues, and merge requested I was able to comment on and approve. **Overall, the collaboration with Jan during the whole project was excellent.**
4. **Assignment finalisation**
   The activity while finishing the thesis was exemplary. I was given the thesis about three weeks before the final deadline, and was also provided with the beta version of the simulator. There was enough time to comment on both the thesis and the software, and to incorporate the most important remarks. I am happy with the final version.
5. **Publications, awards**
   The outcomes of the this thesis have not been published yet, however, the software will be published as open source.
6. **Total assessment** **excellent (A)**
   Jan Vavra was a proactive, enthusiastic and well motivated student who enjoyed the development of this superscalar processor simulator. **The outcome of this thesis is excellent.** It will be a pleasure to employ it as a visual aid in teaching complex processor architectures. The source codes and documentation reaches professional quality an will serve as a platform for future extensions. **Not only do I give this thesis an excellent mark, I also recommend it for the Dean's award.**

In Brno 25 May 2021

Jaroš Jiří, doc. Ing., Ph.D.
supervisor